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Brand:	**Lexicon**
Model	**224**
Product:	**Digital Reverb**
Description:	**Service Manual**

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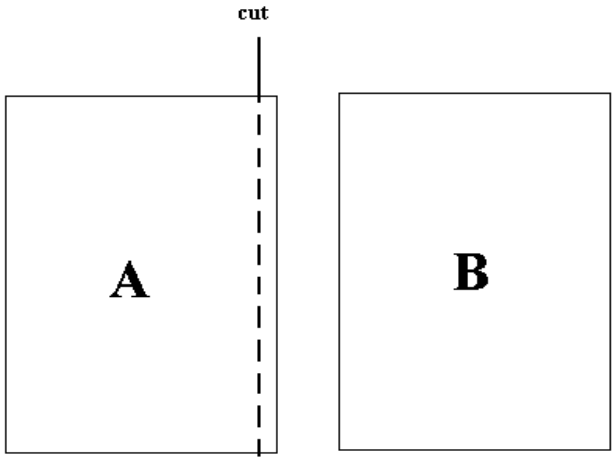
Two Sheet Pasteup Guide

11x17" paper size



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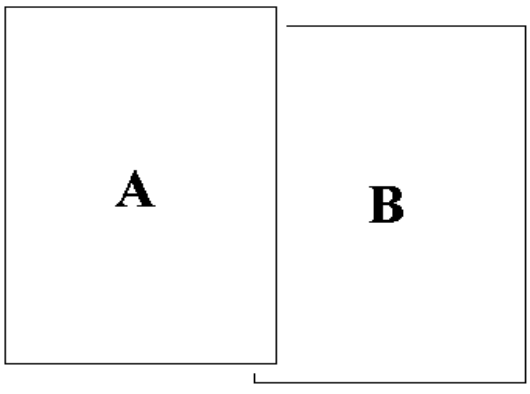


Only one trim cut is needed, then overlay as shown and tape.

MODEL 224
SERVICE MANUAL

1 July 80

IN CASE OF DIFFICULTY....

UNIT WILL NOT POWER UP : FUSE REPLACMENT

If the Model 224 will not power up, first check the line cord for a good connection and the service outlet for power. Next check the power fuse above the service outlet in the mainframe. If the fuse is blown, replace with an exact replacement fuse: 3AG 3A slow blow for "100/120" Volts operation, 3AG 1.5A slow blow for "220/240" Volt operation.

Power Supply Fuses

The 224 contains one low voltage ac plus six separately regulated power supplies. Each supply has a fuse or fuses for circuit protection and safety. If an internal fuse blows it usually indicates the presence of a problem. If failure of any internal fuse is experienced, it is only advisable to consult with a qualified service person.

The following is a list of internal fuses and their location within the machine. Fuses should always be replaced with fuses of the correct rating to insure protection from circuit damage and fire.

FUSE LOCATION TABLE

Supply	Quanity	Fuse Current	Type	Location
+5 Volt	1	15 AMP FAST	3AG	Printed circuit Card adjacent to Fan
-5 Volt	1	2 1/2 AMP SLO	3AG	''
+/-12 Volt	2	3 AMP SLO	3AG	Horizontal Printed Circuit Card attache to heat sink
+/-15 Volt	2	2 AMP SLO	3AG	Vertical Printed Circuit Card attache to heat sink
10V AC	1	2 AMP SLO	3AG	Printed Circuit Bd. attached to rear of remote conn.

Power Supply Verification

In the event of improper operation it is essential to verify the proper operation of all power supplies as a first step in equipment repair.

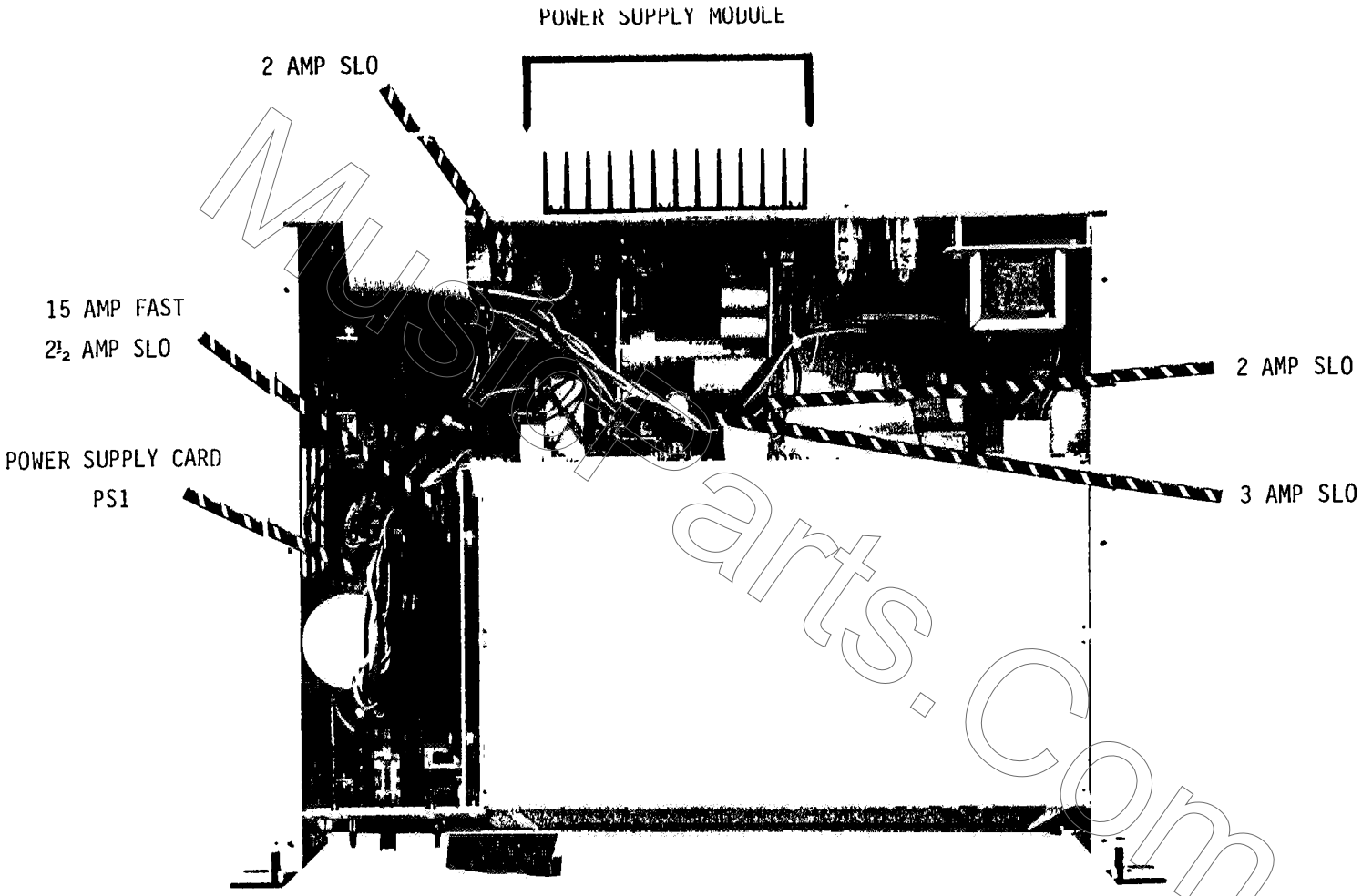


FIG. 1 TOP VIEW-INTERIOR

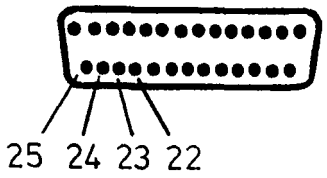


FIG. 2 25 PIN CONNECTOR DETAIL

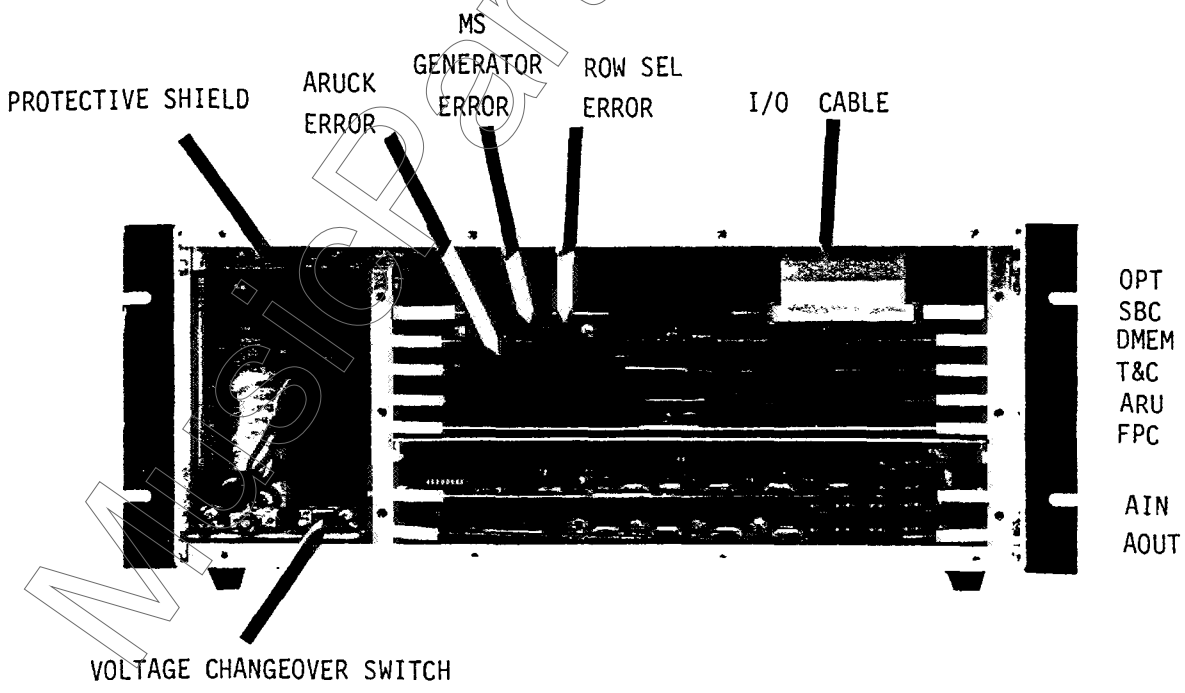


FIG. 3 DIAGNOSTICS AND SELF-TEST

The following is a list of Test Points and voltage tolerances for each power supply. Probe with extreme caution so as to avoid damage to IC's and or supplies. The Chassis can be used for a ground return unless otherwise noted.

SUPPLY	LIMITS	TEST POINT LOCATION
+5 V	4.75-5.25	BLC/SBC BD.; U16, PIN 16: LEFT FRONT-MOST IC; LEFT FRONT IC PIN
-5 V	4.75-5.25	D-MEM BD.; U1, PIN 1: RIGHT FRONT-MOST IC; RIGHT FRONT IC PIN
+12 V	11.4-12.6	BLC/SBC BD.; R8 FRONT LEAD; 2.7K 1/2W RES., LEFT OF R4 (SEE FIG. 3 AND 5)
-12 V	11.4-12.6	BLC/SBC BD.; R4 FRONT LEAD; 82 OHM 1W RES., LEFT OF U15 (SEE FIG. 3 AND 5)
+15 V	14.75-15.25	ANALOG-IN BD.; "+15" TEST POINT; GND TO "⏚" TEST POINT
-15 V	14.75-15.25	ANALOG-IN BD.; "-15" TEST POINT; GND TO "⏚" TEST POINT
+7 V	6.3-7.7	ANALOG-IN BD.; "+7" TEST POINT; GND TO "⏚" TEST POINT
-7 V	6.3-7.7	ANALOG-IN BD.; "-7" TEST POINT; GND TO "⏚" TEST POINT
+7 V	6.3-7.7	ANALOG-OUT BD.; "+7" TEST POINT; GND TO "⏚" TEST POINT
-7 V	6.3-7.7	ANALOG-OUT BD.; "-7" TEST POINT; GND TO "⏚" TEST POINT
10 V AC	8-12V AC	PINS 22/23 TO PINS 24/25; REMOTE JACK, SEE FIG. 2, (25 PIN CONNECTOR DETAIL)

DIAGNOSTICS AND SELF TEST

The 224 contains a number of diagnostic aids to allow identification of defective modules for field repair. The primary diagnostic systems are:

1. Software Diagnostics
2. Diagnostic Indicators
3. Self Test

Diagnostic Programs (operating system V2 and later only)

Model 224 Resident Diagnostics are run whenever the machine is turned on or reset. They may also be entered by holding the "SHIFT" key and pushing the "DEPTH" button. The diagnostics make a single pass through all testable features of the machine. If the machine passes, it commences normal operation. If an error is detected, an error message is displayed.

During an error display or the panel test display all controls and buttons on the panel are inactive except the program switches. Briefly pressing "PROGRAM 1" will stop the display and go to the next diagnostic test. Pressing "PROGRAM 2" bypasses all further diagnostics and starts the regular system.

A stereo delay line program is provided which can be used for setting output levels, or as a quick test of the machine. This program is reached by pressing "PROGRAM 8" while the remote panel test is running, or by pressing "SHIFT" and "PRE-DELAY" during normal operation. The delay is about Ø.4 seconds and is not adjustable.

The diagnostics test the whole machine, including the SBC/BLC computer. To do this they must erase the program numbers and parameters stored in the four registers A through D. These registers must be reset after diagnostics.

Diagnostics make the following tests:

E00 to E0F	Rom checksum
E10 to E13	Computer RAM test - destroys the contents of all registers
--	Remote panel test - all leds illuminated for 2 seconds and operating system version number displayed
E20 to E49	T&C board tests (may also implicate circuits on DMEM)
E51 to E8F	ARU board tests (T&C failures will usually cause ARU and DMEM errors too)
E91 to E93	Data Memory test (DMEM)

All the diagnostics work by comparing the actual data in some part of the machine to the data which should be there if the machine were working perfectly. The diagnostic programs display the expected data pattern (the "good" data) on the lights in the program buttons. The actual data returned by the machine are displayed on the mode-register lights. Usually an error is displayed when the two patterns do not correspond. The pattern displayed on these lights is vital to interpreting the cause of error. If errors appear you should write the error numbers and the light patterns in the order in which they occur prior to contacting Lexicon's custom service department.

Error displays may occur which do not indicate a fault in a vital part of the 224. For example, there may be a problem in the error detection circuits themselves. This is especially true if the only errors which display are T&C errors. On the ARU card, E80 would indicate a possible fault in the overload display circuit, but if no other ARU errors occur the machine may sound fine. If there are several ARU errors or a DMEM error the machine is probably faulty, even if it sounds OK. An error may be occuring in a low order bit which is not easily audible.

Errors are also possible which affect the sound of the machine without causing diagnostic messages. If you are hearing serious noise in reverberation and/or the delay line diagnostic the machine may have problems with the FPC or analog boards. These can be tested with the Self Test feature.

If the boards appear to work in self test, there may be an intermittent on one of the other boards. The diagnostics are only run through the machine once, and they may not pick up an intermittent error. Contact Lexicon for help.

Diagnostic Indicators

Timing and Control Card

The T&C card contains a single LED diagnostic indicator labeled ARUCK ERROR. If this indicator illuminates, it indicates the absence of timing signal ARUCK. This failure would indicate a failure of clock circuitry contained on the T&C card.

Data Memory Card

The D-MEM card contains two LED diagnostic indicators. The leftmost LED labeled "MS GENERATOR ERROR" monitors the period of signal MS2 with one or more of the signals, MSØ through MS7 or MC. This problem could be on either the T&C board or the D-MEM board.

The second LED is labeled "ROW SELECT ERROR". If this indicator illuminates, it indicates a failure of the memory control signals "ROW SEL", RAS/,MC and MCB.

Self Test Mode

Self test mode allows the 224 analog and digitizing sub-systems to be exercised without any intervention from the digital signal processing hardware. This mode digitizes analog information from the left input, and outputs the information to outputs "A" and "B", the right channel input being passed to outputs "C" and "D".

This mode of operation is a meaningful test of the Analog Input, Analog Output and FPC cards.

To activate self test mode the D-MEM, T&C and ARU cards must be loosened from their connectors. It is not necessary or desirable to remove these cards but only to free them from their edge connectors.

The SBC/BLC board has to remain in place in order to provide a clock signal to the FPC card.

Self test exercises about 95% of the Analog In and Analog Out cards circuitry and about 85% of the FPC's logic circuitry. Self test can also be used to test audio throughout performance-set operating levels in the event that a delay line program is not available.

SYSTEM TROUBLESHOOTING (To be included in future update)

RETURNING UNITS FOR REPAIR

Should the Model 224 require servicing, it may be necessary to return a module or machine to Lexicon. Bear in mind that Lexicon assumes no responsibility for units in shipment from customer to factory, whether in or out of warranty. It is important, therefore, that shipments be well packed (in the original packing cartons if applicable), properly insured and consigned to a reliable agent such as UPS or Federal Air

Express. Be sure to include (in the carton) a note explaining the nature of the problem, referencing any conversation with Lexicon personnel, detailing the preferred return shipment method, and indicating a date when the unit is needed again. It is also important to provide us with the name and telephone number of a person we may contact should any questions arise.

MODULE EXCHANGE PROGRAM

In the event that a defective module is clearly identified, Lexicon can usually provide a repair/exchange module in advance of receipt of the defective module. For warranty repairs, Lexicon will ship prepaid by UPS, UPS Blue Label or US Air Mail. If faster turn-around is needed, Lexicon can ship by Federal Air Express or other expedited air service, usually resulting in 24 hour delivery if the customer is near a major airport. In the case of an expedited shipment, however, the customer is expected to pay shipping.

In order to ship a module it is necessary to protect it from static and to provide an adequately cushioned package. Lexicon will provide a static protective bag and appropriate packing materials upon request. A nominal fee for this service will be included in the shipping and handling charges. As an alternative it is also acceptable to wrap the module in aluminum foil and to ship it in a thoroughly cushioned carton.

To remove a circuit board module first loosen the captive screws on the mainframe and remove the front panel. Locate the board, then position the thumbs under each of the nylon "extractor" flanges on either side of the board and pull outwards. The board should then be loosened and will easily slide out. To refit the board, slide it into its track and push firmly on the nylon extractors until it is well seated.

Special Instructions for SBC Boards

The module shipping procedure will be used most frequently for the module in which the programs are contained. That module is the "SBC", a board at the top of the circuit board cage. When returning an "SBC" module be sure to indicate what changes or additions to the programs are desired.

The Single Board Computer "SBC" board can be installed in either the OPTION or SBC slot; this is the only module for which this is true. Every other module must only be placed in its assigned slot.

The SBC board will have at least one ribbon cable edge connector attached to the front edge of the card. These connectors must be unplugged and held out of the way while extracting the SBC card. Do not allow any components on the SBC board to catch or be damaged by these connectors. Place the SBC board in a static protective bag or foil immediately.

2716 Music Program ROM Replacement

Remove ROM(s) to be replaced using an IC extractor or, if not available, pry up each end using a small screw driver. Be absolutely certain that pins of removed ROM's do not get bent or damaged. Immediately place removed ROM's in conductive (black) foam to prevent electrical damage.

Before installing new ROM's identify pin one of the socket and the ROM IC. Failure to install correctly will always destroy the ROM.
NOTE: Install ROM's in the following order:

U23	U24	U25	U26
Vx.x-1	Vx.x-3	Vx.x-2	Vx.x-4

The order is NOT 1, 2, 3, 4. It is 1, 3, 2, 4.

Align all pins before pressing the chip into its socket. Broken pins are not covered by warranty. Refer to the attached figure for location of ROM's on the SBC/BLC computer board.
NOTE: Pin one on the 2716 ROM chip is indicated by a 1, ●, □, ◇ or similar marking. If pin one is not marked, the pin one end of the IC will have a small half circle cut out. See below. The socket will also have a similar marking to indicate pin one's location.

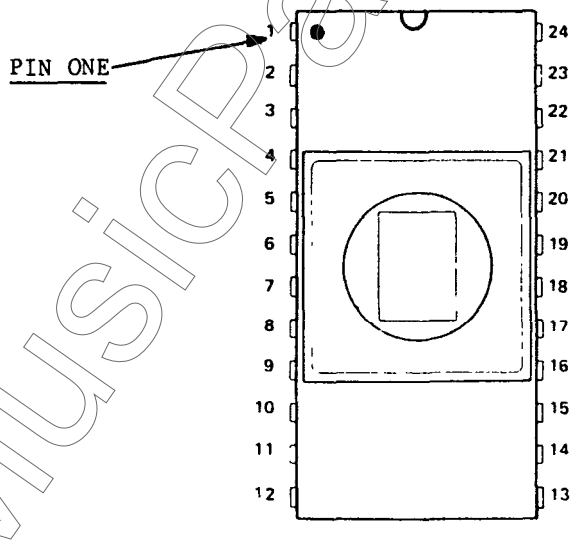


FIG. 4 ROM OUTLINE

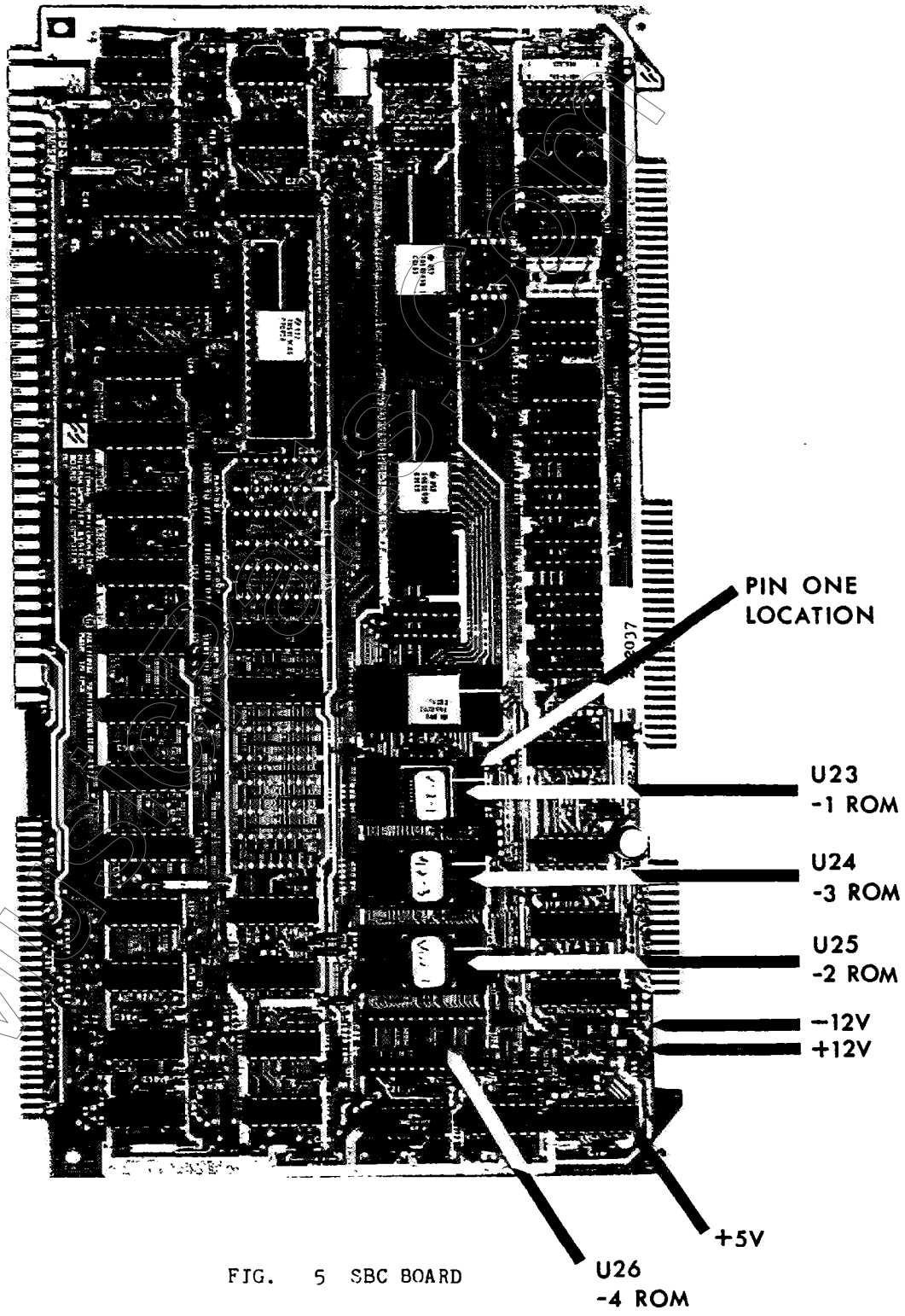


FIG. 5 SBC BOARD

All removed ROM's must be returned to Lexicon for erasure and re-use. ROM's not returned or received in damaged condition will be billed at $150.00 each.

Hardware ECO for Version 1 to Version 2 Conversion

Version 2 software includes a decay optimization which adjusts parameters in the reverberation program in response to changes in input level. Without this ECO the SBC/BLC board causes the digital processor to pause for 500 nano-seconds each time a parameter is changed. This pause can be audible with a sinewave input. This ECO allows the SBC/BLC board to make changes in the reverberation program with no pause, and reduces the audibility of decay optimization on pure tones. Version 1 software will not run properly on a modified machine. Clicks will be produced when the reverberation time sliders are adjusted.

The ECO is very simple: disconnect pin 1 of IC 36 on the T&C card.

In detail:

1. Unscrew the front cover and remove the card labeled T&C.

2. Locate IC 36, a 74LS08 14-pin IC.

3. Carefully remove it from its socket, and locate pin 1. Pin 1 is identified by a small circle on the top of the IC, or by a dimple on one end. (See figure 4).

4. Bend pin 1 away from the body of the chip and reinsert the chip in its socket. Pin 1 should not be in the socket.

5. Be sure the chip has been installed in the correct orientation, with pin 1 facing the front of the board.

6. Reinstall the T&C card and the front cover.

6.6 REPLACEMENT MODULES

Replacement modules and service manual may be ordered from:

Lexicon, Inc.
60 Turner St.
Waltham, MA 02154
U.S.A.
Attn: Parts Dept.

Modules will be shipped FOB Waltham. Prices charged will be those in effect at the time the order is received. Lexicon may be consulted at any time for a quotation.

When ordering modules give a complete description and give the following information.

A. Module type: SBC, DMEM, T&C, ARU, FPC, AIN, AOUT
B. Quantity desired
C. Detailed instructions for programs desired if module is "SBC"
D. Model 224 serial number, if available

DIAGNOSTICS

June 5, 1980

DIAGNOSTICS

Introduction

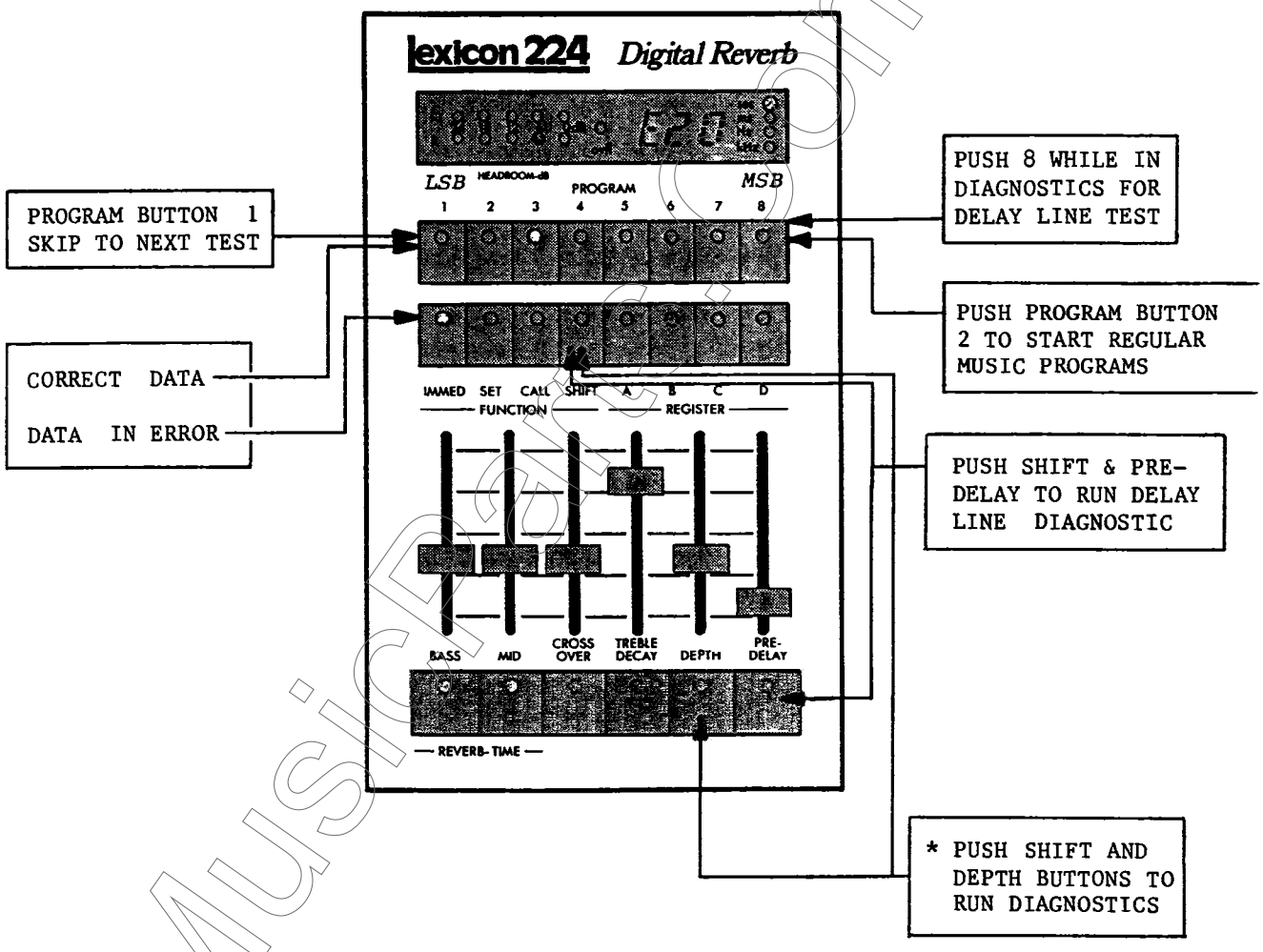
The music program ROM's contain diagnostic test programs which allow a reasonable test of the digital hardware in the Model 224. Although it is not always possible to have a diagnostic program point out the exact component failing it, it is reasonable to expect that a failing section or board can be isolated. Understanding the diagnostics error messages is aided if the overall 224 operation is understood. A basic understanding of the Hexidecimal numbering system is required as well as some knowledge of micro-processor terminology and components.

The following table and figure is provided to aid those not familiar with the hex system and to show how errors and cored data are displayed on the front panel.

DECIMAL	HEX	BINARY
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111
16	10	10000
.	.	.
.	.	.
255	FF	1111 1111

* DIAGNOSTICS RUN WHEN:

1. MACHINE IS TURNED ON
2. RESET BUTTON IS PUSHED
3. SHIFT & DEPTH ARE PUSHED



ERROR DISPLAY ON CONTROL HEAD

Using the Diagnostics

224 Resident Diagnostics are run whenever the machine is turned on or RESET. They may also be entered by holding the SHIFT key and pushing the DEPTH display push button. The diagnostics make a single pass through all testable features of the machine. If the machine passes, the regular Reverb software comes up. If an error is detected, an error message is displayed.

During an error display or the panel test display all controls and buttons on the panel are inactive except the PROGRAM buttons. Pressing PROGRAM button 1 will stop the display and go to the next diagnostic test. Pressing PROGRAM button 2 bypasses all further diagnostics and tries to start the regular system. (Actually any button besides 2 and 8 will start the next test.)

There is a delay line program, which can be used as a quick test of the machine, or for setting input-output levels. This program is reached by pressing PROGRAM button 8 while the remote panel test is running, or by pressing "SHIFT and DELAY" from the regular system.

Diagnostics make the following tests

E00 thru E0F	ROM checksum
E10 thru E13	BLC RAM test - destroys the contents of all registers
—	Remote panel test - all leds illuminated for 2 seconds
E20 thru E23	Program Memory test - T&C Board
E30 thru E49	T&C ports tests
E51 thru E7F	ARU REGISTER tests - ARU Board
E80 thru E8F	Multiply tests - ARU Board
E91 thru E93	Data Memory test - DMEM Board

General Comment

Considerable thought has gone into the order of these tests. In general, if the diagnostics give an error, the source of the first error should be found before a lot of time is spent worrying about the others. All the diagnostics work by loading the program memory with some simple program, and testing the effects of this program on the machine. If there is any problem with program memory, or the decoding of program memory (ports), the rest of the diagnostics will generally give errors even if the sections under test are ok. Some

parts of the tests are impossible to separate. The ARU register test assumes the machine can multiply by one. Likewise, the multiply tests assume that the ARU storage registers work, at least for the default address (all register address lines high).

There is another source of error which may be spread between several boards. Some of the ports used to test T&C are on DMEM, and the decoding for the 8080 bus is also on DMEM. Errors in decoding or in return of ready will make the program memory test take a very long time to complete. The error displayed will probably be E23. The long delay implicates DMEM. Most of the ports tested are physically located on DMEM. Thus they test both the T&C decoding and the bus which transfers this data to DMEM, ARU, and FPC. A short or a defective IC on any of these boards can cause the error. If these errors are seen on a field machine it might be a good idea to have the customer unplug the FPC and ARU boards to see if the error still occurs.

What if the machine does not appear to work at all? The cable to the Remote Panel should be checked first. If there are no diagnostics errors the machine will eventually run reverberation with the remote head unplugged. If the machine does this, the Remote Panel or the cable is faulty. It is however more likely that the transformer plug in the power supply has come loose, or that a power supply fuse has opened. The Self Test mode can be used to check the audio boards and indirectly the power supplies. Self test does not check the +12V or the -5V supply. See the owners manual for Power Supply test points. Failure of the machine to respond either with diagnostics or reverberation when the power supplies are good probably means that the SBC/BLC board has failed.

Detailed Description

E00 thru E0F

Each ROM installed in the 224 is checksummed so that the sum of all the data bytes is zero. The first run diagnostic tests this, and if it finds an error it will display the codes E00 thru E0F depending on which ROM is faulty. The ROM'S are numbered with ROM #1 (U23 - BLC Board) corresponding to bit zeros ROM 2 to bit 1, etc., eg,

	E01 ----------	0001	ROM 1 Bad
	E0F ----------	1111	ROMs 1,2,3,&4 Bad
	E0A ----------	1010	ROMs 2 & 4 Bad

Remember
ROM 1 - U23
ROM 2 - U25
ROM 3 - U24
ROM 4 - U26

NOTE: A checksum error will not always be fatal to proper machine functioning.

E1Ø thru E13

The BLC RAM is tested with a semi-random pattern. Thus all contents are altered. The error display is E1Ø to E13 depending on the address of the bad byte. 1Ø represents 3CØØ to 3CFF, 11 represents 3DØØ to 3DFF etc. The correct pattern is displayed on the PROGRAM LEDs, and the incorrect pattern is displayed on the mode-register LEDs. Any non-corresponding bits should point to the problem.

ERROR CODES

E1Ø = 3CØØ - 3CFF
E11 = 3DØØ - 3DFF
E12 = 3EØØ - 3EFF
E13 = 3FØØ - 3FFF

BIT MAPPING

	LSB 1	2	3	4	5	6	7	MSB 8	
PROGRAM LEDS	0	0	0	0	0	0	0	0	CORRECT DATA
MODE LEDS	0	0	0	0	0	0	0	0	DATA IN ERROR
BIT NO'S	Ø	1	2	3	4	5	6	7	(Note Bits Ø-3 are in U36 of BLC 8Ø/11, 4-7 are in U37)

The test is done in two passes. The memory is loaded with the contents of ROM 1, starting from location zero. It is then complemented twice in two seperate passes. The data in RAM is then compared to the original data in ROM. Data is read from the top down. If the memory is all bad, the test will display E13. Unfortunately the test stops as soon as any error has been detected. If E13 is seen it may mean the whole memory is bad, but in this case it is doubtful that the board or the panel would work at all. This type of RAM test is sensitive to addressing errors and data errors, and will catch every fault except an intermittent error.

PANEL TEST

The panel test simply outputs data to the control head to illuminate all LED's with the exception of the 7-segment displays which will display the revision number of the resident software. The test will be bypassed if PROGRAM button 1 is pressed.

In the event that the panel goes blank after panel test, the following should be considered.

Failure of the DMEM and T&C to return ready to the BLC will cause the program memory test to take over a minute to complete - see below. If the machine still won't come up after several minutes, the protect circuitry on T&C may be holding the 8080. This condition means either that the HALT decoding circuitry on DMEM is bad, or that the protect gating on T&C is bad. There is no way to tell which without swapping boards.

E20 thru E23 Program Memory

The program memory (U3, U18, U33, U48 and associated circuits on T&C Board) is tested the same way as the BLC RAM memory. Errors are displayed as E20 to E23.

E20 - Locations 4000, 4004 .... 41FC (U49 & associated circuits)

E21 - Locations 4001, 4005 .... 41FD (U33 & associated circuits)

E22 - Locations 4002, 4006 .... 41FE (U18 & associated circuits)

E23 - Locations 4003, 4007 .... 41FF (U3 & associated circuits)

Good data is on the program LED's, bad on the mode-register LEDs. An error of 23 may mean the whole memory is bad. If it is, or if a problem on DMEM prevents data from being properly loaded in to the program memory, the memory test will take a long time to complete. Such a delay implicates the BLC buss decoding ckts on DMEM or on T&C. If the machine is in the field and the customer is known to be competent, two of the memory chips can be swapped to see if the error displayed is different. There are other problems which can cause a bad program memory. The address lines may be open or shorted, or the address or data buffers may be defective. The diagnostic will detect this, but it takes a more sophisticated test to identify the source of the problem. The BLC monitor program can be used in conjuntion with an external computer to write and read a single location. If this works, the addressing is probably bad. If it does not, suspect the chip or the data buffers.

E30 to E49 General Description

Many tests are performed on the T&C through the ports. Errors are displayed: E30 to E39 input port errors, E40 to E47 output port errors. As usual the LEDs show the good and bad data. An error here must be checked against the port definition to determine the meaning. Remember the ports test checks the condition of the control bus as well as the decoding circuits. Unplugging ARU and FPC may help diagnose a problem.

E32

The 8080 bus test register is checked first. The error number is E32.

Error here means the 8080 cannot communicate with the HSP. If the error is real it is fatal both to further diagnostics and to reverberation. Shorts on T&C or DMEM may be at fault. Check to see if the error occurs with T&C unplugged. If it does, DMEM, the Back-Plane, or the SBC/BLC is at fault. If the machine appears to work in reverberation in spite of this error, the error can be ignored. U34 on DMEM (the bus test register) is faulty.

E43

This is followed by a test that the HSP can read and write the XREG E43. To make this test the diagnostics load the program memory with a NOP in step zero, and an instruction to read the XREG and write the XREG in step one. If the processor can not perform this function it means the XREG itself may be bad, or the decoding of the bus control bits of the T&C card does not work. It is important that these errors be fixed before further diagnostics are interpreted, since an invalid XREG transfer may give incorrect results in the halt test which follows, and further invalidate the whole next sequence of tests. This error may indicate shorts or bad chips anywhere on the DAB. If the machine is in the field ARU and FPC should be unplugged to be sure there is no bad component on them pulling down the bus. DMEM may also be at fault, but no tests work with DMEM unplugged.

E40 & E41

E40 and E41 provide tests of the halt and single step modes of the machine. (Out 0 and Out 1, or E40 and E41) Both tests will give an error if the data returned match, indicating the machine refuses to halt. It is essential that the machine halt if the following dignostics are to be correct. The 224 halts by continually repeating the first program step. Most of the ports tests work by loading known data into the first program step, and then looking for that data at the output of the T&C. If the machine does not halt all the further tests will be false. The machine may sound fine. The halt test works by loading an instruction in the program memory second step which transfers data from the XREG input to the XREG output. It then loads the XREG with something, and checks to see if the same thing comes out. If the machine does not halt the data will be the same. Saturation is not tested in the ports test. The multiply test will check it.

E31 and E80 on earlier machines

The ports tests may show several errors on a machine which works fine. This will be especially true on machines shipped before the diagnostics were used in checkout. Faults in any of the circuits used for diagnostics will cause non-fatal errors. The most common ones at the time of this writing (and you will see a lot of these) are E31 with PROGRAM lights 7 and/or 8 incorrect, and E80. Both errors are due to bad 74LS123's. E31 implicates U13 on DMEM, a one-shot used to stretch the transfer and case signals for diagnostic purposes only. E80 is non-fatal, but should be immediately fixed. It indicates the saturation (overflow) monostable does not work, and will cause the user to overdrive the machine. The new software also uses the Protect feature of the machine, for which there is no diagnostic. It is possible that machines prior to serial 2102 may have bad protect circuits. This will be shown by these machines making excessive clicking when the "Decay Optimization" sub-program is used after making the recommended field ECO to U36 on T&C. If this ECO causes an increase in the clicking when the reverb time controls are varied (with the new software only) protect does not work and the ECO should not be performed until the T&C can be returned for service.

E51 to E7F: ARU RESISTER TESTS

To properly test the ARU REGISTERS you must assume the multiplier can at least multiply by one. This may not be the case. To help sort things out all addresses of the REGISTERS are tested. E50 to E5F indicates the low byte is bad, and the bad register address is given by the 0 to F. Thus E51 means only address one of the low byte is bad. Each address is represented by the corresponding bit, so address 2 only bad would give E52. Both one and two bad give E53 etc. If the high byte is bad the error display will be E60 to E6F, and if both bytes are bad the display is E70 to E7F. To see how this helps, assume:

A. The multiplier is OK and the RESISTERS are bad.

1. If both high and low bytes are bad the register addressing is probably not right. This should result in an error on some registers and not on others.
2. If there is a bad file chip only one byte will be affected, and only part of that byte. It may affect all addresses or just one. The data on the LED's must be checked to determine which chip.

B. The REGISTERS are OK and the multiplier is bad.

1. Here all addresses of the files should give an error, but it may or may not be confined to one byte or set of bits. In any case replacing the suspect chip will not correct the error.

E80 to E8F Multiply

This tests the ability of the multiplier to work correctly. If the REGISTER test is OK you know it can at least multiply by one, and this may be a help. The multiply test is in four parts, each of which display their error separately. E81 to E83 indicate an error when the multiply coefficient is -010101. E81 indicates a low byte error, E82 a high byte error, and E83 indicates both errors. E84 to E87 indicate an error in multiplying by +010101. E88 to E8A indicate an error in the coefficient -101010, and EC to EF indicate an error with coefficient +101010. Four multiplications are made with each coefficient. The bad data and the correct data are shown as usual. If both the high byte and the low byte are bad, the data shown are the low byte data. E80 indicates an error in the saturation monostable. The last two coefficients should set it. An error is given if it is not set. If a multiply error is displayed before this test the monostable may have cleared before it is tested, and a false error given. The monostable is only tested for the set condition. Failure to clear will result in the panel light being permanently on, which is visually obvious.

The multiply test is not complete as of this writing. It does not exercise the coefficient 110000 or the proper data to detect an error in the first set of adders. Thus a machine can pass diagnostics and still have a hard error in multiply which will raise the distortion level in reverberation mode (but not delay line mode.)

E91 to E92 Data Memory Test

This is similar to the old MEMTST routine, except that it makes only two passes with complementary data. Display is E91 for low byte and E92 for high byte. It also assumes the multiplier works. If both bytes are bad the test will display only 91, and this error may mean

the memory is totally bad. It may also mean the multiplier or T&C is bad. The memory test is sensitive to both data errors and addressing errors, and should catch most problems. If E91 or E92 is the only error displayed and only a single light is incorrect the problem is almost always a memory chip, and the chip can be identified from the lights. If the machine is in the field the defective memory can be swapped with the lowest order memory chip (U1). This will increase the noise level of the machine by 6dB but put it back in service.

PANEL LED'S — "1"	"2"	"3"	"4"	"5"	"6"	"7"	"8"
BIT NO. — 0	1	2	3	4	5	6	7

CODE	PORT								
E40/	OUT Ø	SINGLE CYCLE MODE							
E41/	OUT 1	CONTINUOUS RUN MODE							
E42/	OUT 2	HALT IMMEDIATELY							
	OUT 3	(NOT TESTED) CONTINUE							
	OUT 4	(NOT TESTED)							
	OUT 5	(NOT TEST.) CLEAR CURRENT POSITION COUNTER							
	OUT 6	(NOT TEST.) WRITE LOW BYTE OF "X" REGISTER							
	OUT 7	(NOT TEST.) WRITE HIGH BYTE OF "X" REG., BUS TEST REG.							
E30/	IN Ø	OFSTØ	OFST1	OFST2	OFST3	OFST4	OFST5	OFST6	OFST7
E31/	IN 1	OFST8	OFST9	OFST1Ø	OFST11	OFST12	OFST13	XFER	CAS
E32/	IN 2	READ BUS TEST REGISTER							
E33/	IN 3	SAT/	$\overline{S\emptyset \oplus S1}$ AS$\emptyset$	$\overline{S\emptyset \oplus S1}$ AS2	$\overline{S\emptyset \oplus S1}$ AS1	C3 ⊕ C2	$\overline{C1 \oplus C\emptyset}$	S5 ⊕ C4	ZERO
E34/	IN 4	WAØ	WA1	RAØ	RA1	CSIGN	RD AD	MEM W	RESET/
E35/	IN 5	SDAA/	SDAB/	SDAC/	SDAD/	WR DA	WR XREG	RD XREG	RD RREG
E36/	IN 6	READ LOW BYTE OF "X" REGISTER							
E37/	IN 7	READ HIGH BYTE OF "X" REGISTER							
E38/	IN 8	CH 1 HEADROOM (NOT TESTED)							
E39/	IN 9	CH 2 HEADROOM (NOT TESTED)							

THEORY OF OPERATION

System Overview

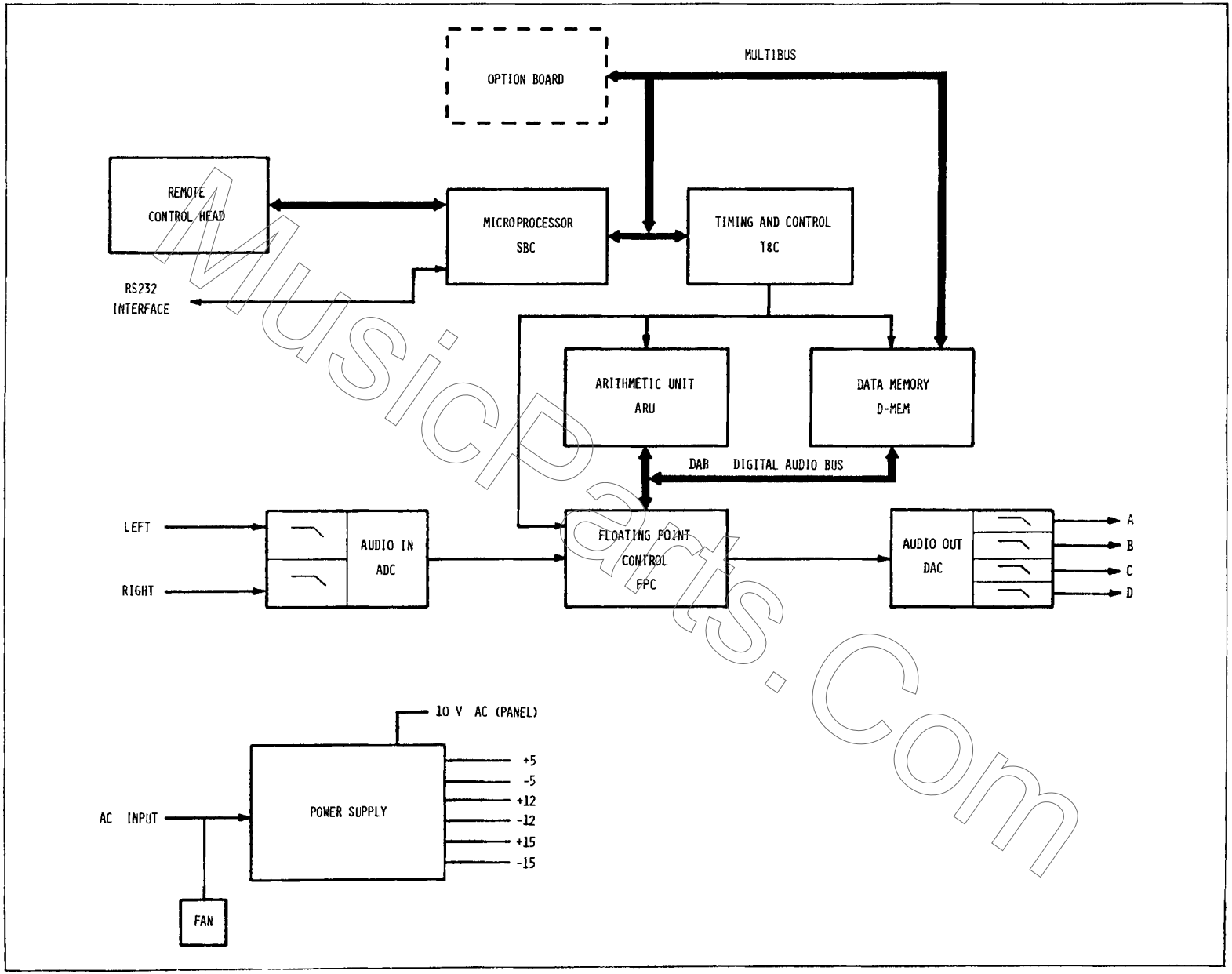


FIG 1 224 BLOCK DIAGRAM

Introduction to Theory of Operation and System Overview

Theory of Operation

The 224 is partitioned into 9 major functional blocks (not including the option module). They are:

1. Single Board Computer - SBC/BLC
2. Data Memory - D-MEM
3. Timing and Control - T & C
4. Arithmetic Unit - ARU
5. Floating Point Converter - FPC
6. Audio Input - A-IN
7. Audio Output - A-OUT
8. Remote Panel
9. Power Supply - PS1, PS2 and PS3

SBC Single Board Computer

The single board computer controls all functions of the front panel such as reading switches, slide pots and display of data. The SBC also contains the 224 music software which is used to control the "Digital Processor". These programs are stored in Read Only Memories, "ROM's". It is these ROM's which have to be re-programmed whenever software is updated.

An RS232 interface is also provided on the SBC board to allow automation interface as well as diagnostic procedures to be executed with no additional hardware. This interface may be set to any data rate between 9600 and 110 baud.

Input/Output Signal Paths

Input analog signals are transformer coupled, gain conditioned and filtered prior to digitization. The input digitizer sequentially converts each analog signal into a digital representation which the FPC card transfers to the digital processor as a 16 bit offset binary word.

The FPC card is also used to process output data to the output DAC. The output DAC circuitry reconstructs the analog information which is then low pass filtered and transformer coupled to the output channels.

Self Test

In the event of operating difficulties it is possible to determine proper operation of the Input, Output and FPC cards by enabling self test mode. This mode is a reasonably good test of Audio

and FPC subsystems. Additional information about self test is obtained in Section 6 of this manual. Self test mode is enabled by loosening the D-MEM, T&C and ARU boards. When these cards are loose a control signal to the FPC card is allowed to fly high placing it in self test mode. It should be noted that the SBC card must be installed simply to provide a clock signal for the FPC board.

Digital Processor

The processor unit consists of three cards, D-MEM, ARU and T&C. These cards provide the basic digital processing and data storage capability to allow the 224 to synthesize reverberant sound in either stereo or monophonic formats.

Remote Panel

The remote panel interfaces to the main frame via a 25 conductor ribbon cable. 10 Volt AC power is sent to the control head where it is rectified, filtered and regulated to power the control head logic. All data sent to and received from the control head is sent over an 8 bit bidirectional data bus. Address data is sent over a 4 bit address bus for pot selection and digit scan. All slide pots are digitized under software control and converted into an 8 bit word for transmission to the SBC/BLC board.

Power Supply

The 224 Power Supply produces six regulated dc Voltages and one unregulated ac voltage to power the control head.

+5 and -5 Volt Supplies

The +5 and -5 Volt supplies are both derived from a single secondary winding. The +5 Volt supply consists of a ua 723 regulator, current boost transistor and a pair of high current pass transistors. The regulator is a current foldback design which will limit short circuit currents to less than 3 amps.

Over voltage protection is provided by a crowbar circuit and the entire supply is fused by a 15 amp 3AG fuse. This supply is designed to provide a continuous 10 amp - both voltage and current limit are adjustable.

The -5 Volt supply is a 7905 monolithic regulator fused at 2.5 amps. This supply is both current limited and thermally protected. It is designed to provide 250ma.

+12 and -12 Volt Supplies

The + and - 12 Volt supplies are both derived from a single secondary fused in both legs by a pair of 2 amp slo fuses.

The +12 Volt supply is a LM317K monolithic Voltage regulator programmed by a pair of 1% resistors. This supply is both thermal and current protected - it will provide 1.25 amps.

The -12 Volt supply is derived from 7912 monolithic regulator which is thermal and current protected - it will provide 150ma.

It should be noted that the +12 Volt supply is sequenced by the -5 Volt supply so that +12 Volts can not come up until after -5 Volts is available. Should any problems occur with +12 Volts the presence of -5 Volts should also be checked.

+15 and -15 Volt Supplies

The + and - 15 Volt supplies are a tracking design which allows the -15 Volts to track the +15 Volt supply. Both supplies are derived from a single fused secondary. The +15 Volt supply is a LM317 programmed with an adjustable resistor network.

The -15 Volt supply is a 7912 controlled by a 301 op amp which senses the +15 and -15 Volt outputs and forces the -15 Volt output to track the +15 Volts. A balance control is provided to trim the -15 Volt output. It should be noted that the +/-15 Volt supply is not ground referenced to the +/-5 and +/-12 Volt supplies unless the analog boards are installed in the 224 chassis. When measuring voltages it is essential to refer all measurements to the correct ground.

The +/-15 Volt supplies will provide 750ma and are current and thermally protected.

Mains Circuit

The mains circuit for the 224 uses a dual primary transformer with 115 and 100 Volt taps - a pair of DPDT selector switches select the operating voltage. This supply is switched on both sides of the line. A primary fuse is provided on the chassis ahead of the RFI filter unit. Fan power is maintained at 115 Volts by placing the fan across one of the 115 Volt primaries.

System Overview

A block diagram of Model 224 is shown in Figure 1. In this diagram, each of the boxes represents a seperate card, and except for the Front Panel cards all cards plug into an 8 slot cage and are interconnected via a motherboard. The three cards designated T&C, DMEM, and ARU comprise a dedicated 500nsec cycle time microprogrammed signal processor and will be collectively referred to as the High Speed Processor.

During normal operation signal flow begins with the 2 channels of audio. These channels are filtered, sampled, and digitized by the Audio INput card (AIN). The Floating Point Converter card (FPC) converts the floating point number (12 bit mantissa, 2 bit exponent) from the Audio Input card, to a 16 bit fixed point two's complement number and transmits it (upon request from the High Speed Processor) over the 16 bit Digitized Audio Bus (DAB) to the High Speed Processor. The High Speed Processor operates on this data and generates up to 4 independent channels of output data. This data is passed back to the Floating Point Converter card which converts it back to floating point form. The Analog OUTput Card (AOUT) reconstitutes four analog signals from the digital data stream.

The 8080 microprocessor card scans the switches and pots and drives the displays on the Front Panel. It is also responsible for loading the writable control store of the High Speed Processor and for changing various parameters in the control store as dictated by changes in Front Panel Control setting. In the case of machine malfunction, the 8080 will be responsible for exercising and diagnosing the High Speed Processor.

Lastly, an Option slot has been provided. Any card plugged into this slot can communicate to the SBC 80 using the standard multibus protocall. Possible option cards include a ROM diagnostic card and a computer interface card.

A more detailed block diagram is shown in Figure 2. Some of the major data and control paths internal to the cards ar depicted.

THEORY OF OPERATION

Data Memory Card

Data Memory Card

From the block diagram in Figure 1 observe that the Data Memory card contains the Data Memory, circuitry which takes care of control signal and address generation, the X Register, diagnostic ports and the 8080 port decoding circuitry.

Data Memory

The Data Memory communicates to the rest of the system via the Digitized Audio Bus. The address coming from the microinstruction is in the form of an offset relative to a Current Position in memory. This Current Position is held by the 14 bit Current Position Counter, U28, U90, and is incremented (in principle) once every sampling interval. The absolute address of a memory reference is computed by subtracting the offset from the Current Position. A true 2's complement subtraction is performed by adding the complemented 14 bit word, OFST/, to the output of the Current Position Counter and tieing the carry input of the adder (U26,27,38,39) high. A 3242, U24, is used to multiplex the resulting 14 bit address onto the 7 address lines of the 16 dynamic RAMs. The address and control lines of all the RAMs are tied together. Because the RAM outputs are capable of fanning out to ten LS-TTL loads they are tied directly to the Digitized Audio Bus without buffering.

The timing and control signals for the Data Memory are generated by gates U11,12 and Schottky flip flops U9 and U10. (Sheet 2 of DMEM schematic) This circuitry has been deliberately located on this card in order to minimize the run lengths of the Schottky memory strobes. Detailed Data Memory timing is depicted in Figure 2. The following is a description of the sequence of events:

1. The Micro Instruction Register on the Timing and Control card is loaded thus updating OFST/, the Data Memory access bit MEMAC is asserted, the Refresh Enable input goes low. The 3242 therefore gates the 7 LSB's of the 14 bit address onto the 7 RAM address lines.

2. After the 7 LSB's have been allowed enough time to settle, Row Address Strobe, RAS/ drops low clocking these 7 bits into the dynamic RAMs.

3. Once address hold times have been met the Row Enable input falls thus selecting the 7 MSB's of the 14 bit address.

4. The RAM address lines are allowed to settle after which Column Address Strobe , CAS/, falls clocking in the second half of the 14 bit address. At the falling edge of CAS/ the control signal MEMW/ is sampled. If it is asserted a memory write takes place and the data on the Digitized Audio Bus must be valid.

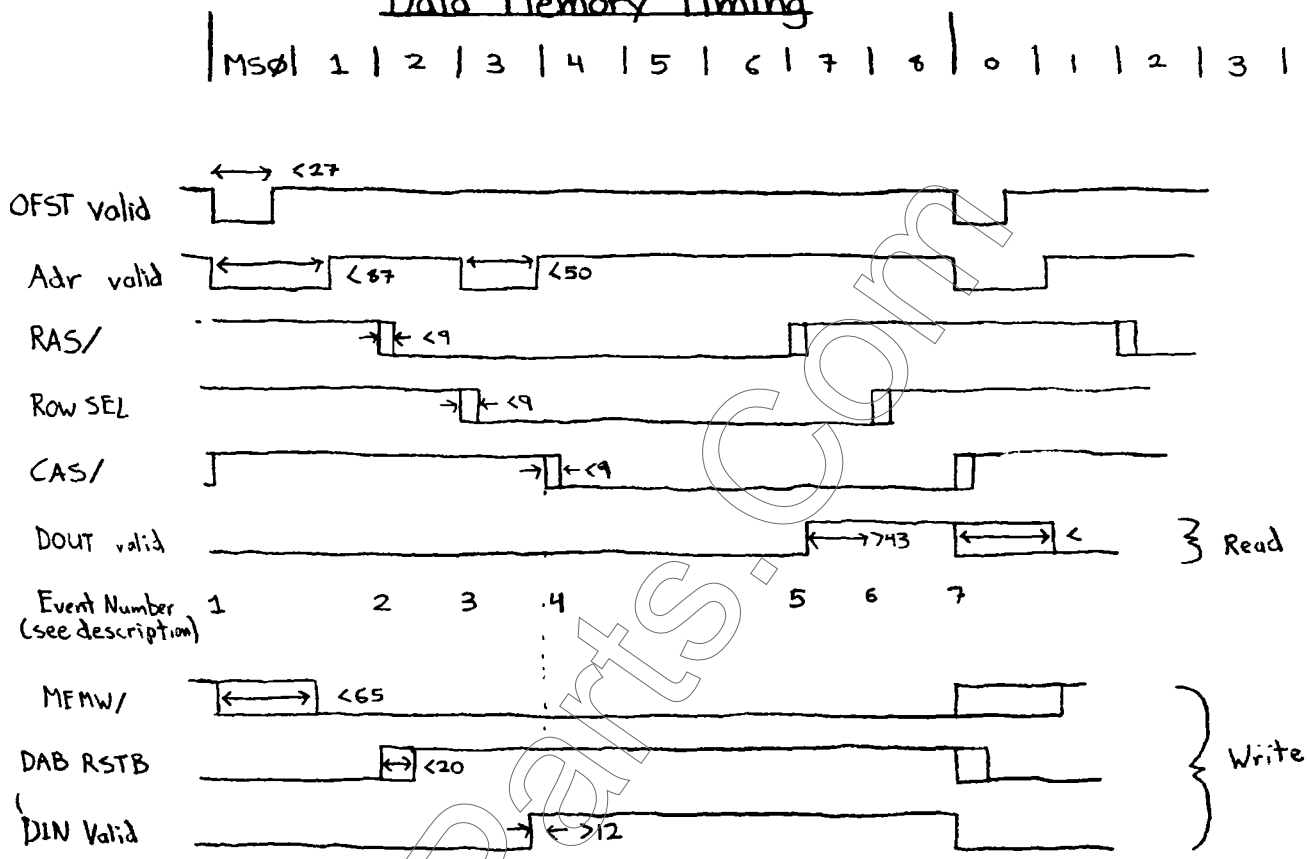
5. RAS/ is deasserted. This has no effect what so ever

6. Row Select returns high. Note that the column address has been latched and need no longer remain stable.

7. CAS/ is deasserted terminating the memory cycle. Note that the RAM may take as long as 80 ns to release the Digitized Audio Bus.

Data Memory Timing

2117-4



Notes:

1. CAS/ falls only when MEMAC is high indicating memory operation
2. critical timing path For DIN is clock to XFER CK to Result Register of ARU

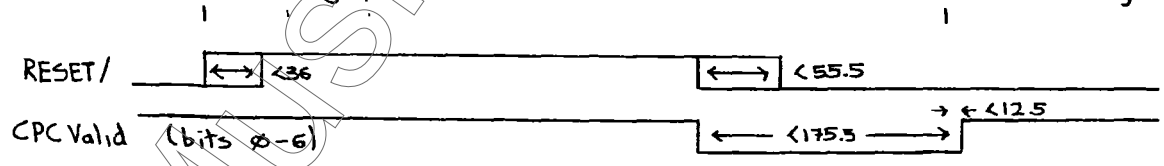


Figure 2
Data Memory Timing

Because the 2117/4116 is a dynamic memory it is refereshed during those icroinstruction cycles which do not access Data Memory. The 3242, U24, contains a refresh counter which will address the RAMs whenever the input Refresh Enable is high. Nand gate U11 ensures that the refresh counter is selected when the High Speed Processor is executing a microinstruction which does not reference Data Memory or whenever the High Speed Processor is halted. During the execution of a non-memory referencing microinstruction, MFMAC, a bit in the microinstruction, will be unasserted inhibiting Flip Flop U9-5 from generating a CAS/ pulse. The resulting RAS/ only memory cycle refreshes the RAMs while inhibiting them from any interaction with the Digitized Audio Bus. Because the refresh counter is clocked by the falling edge of MS2, the count is updated every instruction cycle just after RAS/ clocks in the Row Address.

The current Position Counter must be updated once every sampling interval. The rising edge of RESET/ from the Timing and Control card is used to clock the counter. This edge has been carefully timed so that the counter update occurs late enough for the current Data Memory access to proceed undisrupted yet early enough for the updated count to be used by the following cycle. (See Figure 2) Remember that only the 7 lower order bits of the address need settle by the falling edge of RAS/ ; the 7 higher order bits have until the falling edge of CAS/ 100ns later!

X Register

The X Register is the sole data path between the 8080 data bus and the High Speed Processor Digitized Audio Bus. Through this register the 8080 and the High Speed Processer may exchange data. Four octal tristate registers are used to implement the Text Register. U30 and U32 are used to transmit data from the High Speed Processor to the 8080, while U31 and U35 are used for transfers in the opposite direction.

8080 I/O Ports

One of eight decoders U45, U46 and U47 are used to generate the strobes effecting an 8080 I/O port operation. U45 decodes the eight output ports, 0- 7, while U47 and U46 decode the ten inputs ports 0-9. Open collector NOR gate U43-1 is responsible for returning an acknowledge, XACK/ back to the 8080.

NAND gates U49-8 and U49-11 are used to implement the SCYCLE-Continuous Run Latch. If SCYCLE is high while a Reset microinstruction is executed the High Speed Processor is placed in the halt state.

Diagnostics

The diagnostic circuitry on the Data Memory card is

comprised of two clock error LED's and three diagnostic ports.

On page 2 of the Data Memory schematic the MS GENERATION ERROR circuit can be found. The circuit monitors the period and duration of MS2 because MS2 is the very last stage of the shift register which generates all the MS signals. Consequently confirming that MS2 is correct is a fairly good confirmation that all the MS signals are good. U14 normally counts:

(LOAD)	1111	MS2
	0111	MS3
	1000	MS4
	1001	MS5
	1010	MS6
	1011	MS7
	1100	MS8
	1101	MS9
	1110	MS1
(LOAD)	1111	MS2
	0111	MS3

The carry output U14-15 is low for eight clock periods and high for one clock period. Carry is compared to MS2 and any difference between the two waveforms causes flip flop U41-9 to go high triggering monostable U52-12 which lights the LED.

On page 1 of the Data Memory schematic the ROW SEL ERROR circuit monitors the period and duration of the memory control signal ROW SEL. Again since ROW SEL is produced by a shift register this circuit effectively monitors RAS/ as well. The normal count sequence for U53 is :

(LOAD)	1100	MS7
	0100	MS8
	0101	MS9
	0110	MS1
	0111	MS2
	1000	MS3
	1001	MS4
	1010	MS5
	1011	MS6
(LOAD)	1100	MS7
	0100	MS8

QD,U53-11, happens to be the complement of ROW SEL. XOR, U29-6, compares the two signals and flip flop U41-5 falls when a discrepancy is detected causing monostable U52-4 to fire lighting the LED.

Tristate drivers U35 and U36 enable the 8080 to read the OFST arriving on the Data Memory card as well as activity in the XFER CK and CAS/ control lines. Bus Test Register U34 enables the 8080 to make a very preliminary test of the external 8080 data bus.

Floating Point Converter Card

The Floating Point Converter card serves as an interface between the High Speed Processor and the Analog Input and Output cards. From the point of view of the High Speed Processor, the Analog I/O looks simply like another device which can be read from and written into via the Digitized Audio Bus. From the point of view of the analog cards, the Floating Point Converter card is the sole source of the timing strobes and clocks which direct the A/D and D/A conversion processes. Additionally the card is reponsible for making the Floating Point - Fixed Point translation required for the two Analog cards to communicate with the rest of the system.

Input

The section of circuitry responsible for controlling the A/D conversion, connverting the floating point number to fixed point representation, and for transmitting the data onto the Digitized Audio Bus occupies the upper half of sheet 1 of the Floating Point Converter schematic. A 256 x 4 bit PROM (U18) handles the generation of the timing signals which control the track/hold, channel select switches, gain range resister, and the successive approximation register on the Analog Input card. The PROM is driven by an 8 bit Input Cycle Counter U7,U8 which is synchronized to the microprogram execution sequence by the Reset microinstruction. Assuming that multiplexer U4 selects the "A" inputs, RESET/ coming from the Timing and Control card gets selected by U4 to synchronously clear the counter thus initiating a new conversion cycle. The Floating Point Converter Clock has been selected to be MS5 in order to ensure that the High Speed Processor signals RESET/ and WR DA/ are sampled at the correct time. Figure 1 depicts the A/D cycle timing; the following is a description of the sequence of events:

A Reset instruction is executed by the High Speed Processor causing, among many other things, the Input Cycle Counter to clear and start a new cycle. The Start Conversion input to the SAR, STCONV/, is brought high and the Conversion Clock of the SAR receives thirteen clock pulses. Just after the twelfth Conversion Clock the SAR contains valid data which is loaded into the shift register U27,U28,U38,U39. STCONV/ is brought low and the thirteenth Conversion Clock clears the data from the SAR resetting it for the following conversion.

Shift Register U27,U28,U38,U39 and counter U16 perform the floating point to fix ed point conversion. Note that LOAD, U6-9, is asserted for two clock pulses. The first clock pulse loads Input Gain Counter, U16, with the Input Gain bits IGA1 IGA0. Because a one is also loaded into QC, U16-12, which is conne cted to the S1 input of the shift register, both S1 and S0 of the Shift Register will be high for the second clock pulse causing it to load the 12 bits from the SAR. When LOAD/ returns low the Input Gain Counter will count up and the shift register will shift left until QC QB QA = 000. Gain bits of 00 will result in four shifts, 01, will result in three shifts, 10, in two shifts, and 11 in one shift. By the fourth clock pulse following the falling edge of LOAD the Channel 2 conversion will be complete. Tristate drivers U25, edge of LOAD the Channel 2 conversion will be complete. 5 U26 will enable this data on to the Digitized Audio Bus when the High Speed Processor asserts the RD AD/ line. Meanwhile CH1L (a signal derived from CH1 on the Analog Input Card) has risen causing an input channel switch. A similar conversion for Channel 1 takes place during the second half of the input conversion cycle.

THEORY OF OPERATION

Floating Point Converter Card

Output

The section of circuitry responsible for receiving a fixed point number from the High Speed Processor, converting it to floating point, and running the D/A conversion occupies the lower half of the Floating Point Converter schematic.

The 4 bit register U40 and the 16 bit register U36,U37 comprise a double buffer which stores the output channel select code SDAA-SDAD, and the 16 bit output value, respectively. When the High Speed Processor signals an output to the D/A by asserting WRDA/, the Double Buffer is loaded and NEW DAT/, U3-6, is asserted indicating that the Double Buffer is full. At the next clock pulse gate U14-13 inspects BUSY, U14-11, from the Strobe Counter. If BUSY is high indicating that a D/A conversion is currently taking place nothing happens. If BUSY is low the 16 bit data stored in the Double Buffer is loaded into shift register U23,U24,U34,U35; the 4 bit Select Code stored in the Double Buffer is loaded into register U41; and the flag NEW DAT/, is deasserted indicating that the information in the Double Buffer has been used. NOR Gate U14-1 ensures that this flag is not deasserted if the High Speed Processor reloads the Double Buffer just as the old information in the Double Buffer is loaded in to the registers below.

When the shift register is loaded Strobe Counter, U1,U2, and Output Gain Counter U43, are loaded initiating an output cycle. (Figure 2) The Output Gain Counter counts up from zero and the shift register shifts left until NOR gate U14-4, detects one of two conditions: 1). The sign bit is about to be shifted out of the shift register (that is the 2 MSB's disagree) When STOP/ falls, the fixed to floating point conversion is complete. or 2). The counter has incremented three times. The two LSB's of the Output Gain Counter are transmitted to the Gain Switchable Attenuator on the Analog Output Card as Output Gain bits OGA1, OGA0. Meanwhile the Strobe Counter has been counting up from its initially loaded value of 2A.(Hex) After allowing enough time for the fixed to floating point conversion to complete and then enough time for the GSA and D/A on the Analog Output Card to settle, flip flop U3 pulses the muliplexer enable pin U43-15 thereby strobing the appropriate ouput line OUTA-OUTD.

Headroom

The headroom circuitry is shown on page 2 of the Floating Point Converter schematic. Because the Headroom lines transmitted by the Analog Input Card are shared by both input channels, the two seperate headrooms are demultiplexed by clocking two Headroom registers on opposite edges of the channel select signal, CH1. Peak detection is accomplished by clearing a register bit any time the corresponding headroom bit is asserted. What remains in the register, then, is the complement of the largest Headroom word which occurred since the register was initialized. The 8080 reads a Headroom

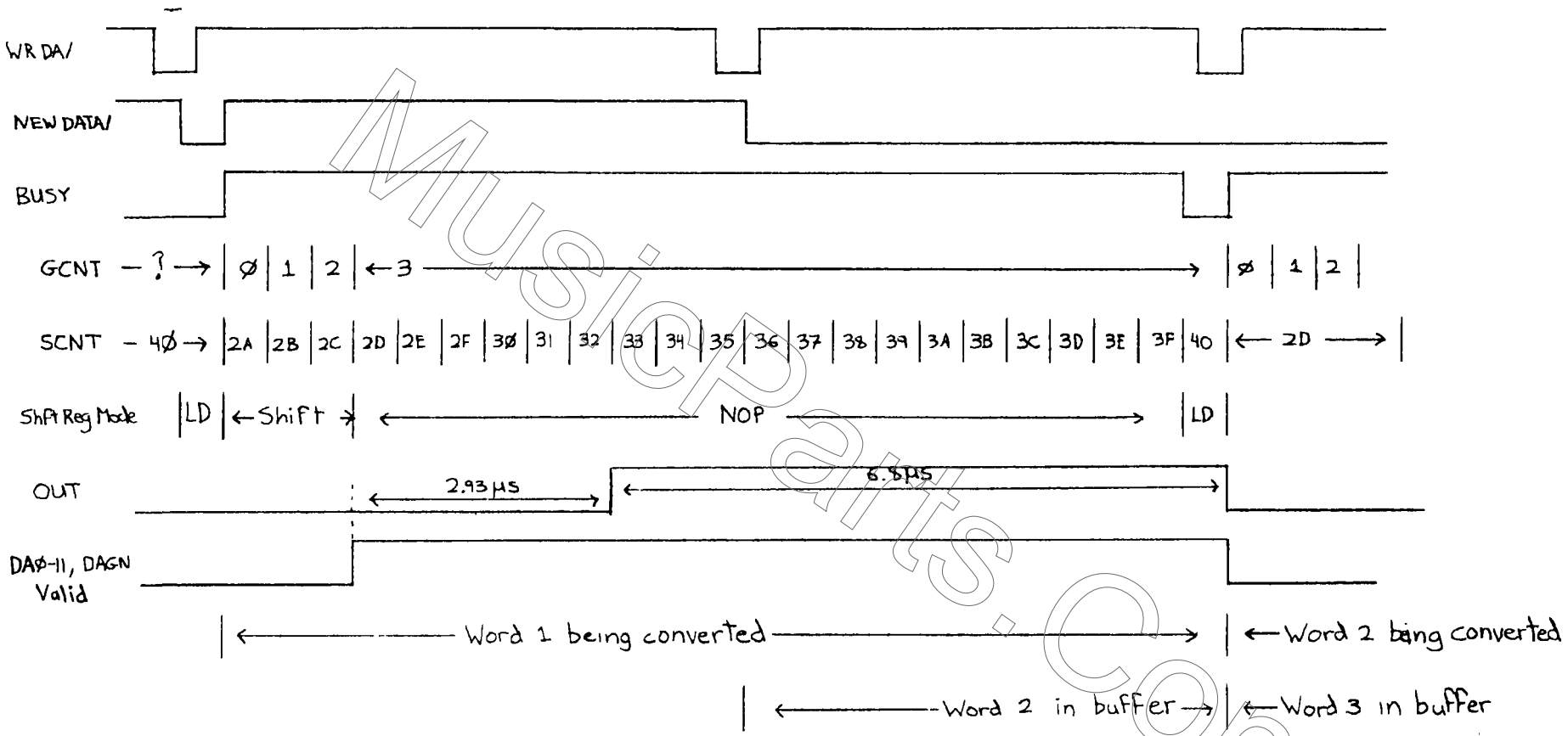


Figure 2
Fix to Float Conversion &
D/A cycle timing

Register by strobing either HR1/ or HR2/ low enabling the tristate drivers A12 or B12 onto the 8080 data bus. The rising edge of the strobe triggers a monostable which presets the corresponding Headroom register.

FPC DEBUG

A feature has been incorporated into the Floating Point Converter card wh ich allows the analog input and output system to run in the absence of any signals from the High Speed Processor. When the ARU, DMEM, and T&C cards are removed, a wired - AND line, FPC DEBUG, floats high causing the Floating Point Converter card to substitute internally generated control signals for those nomally driving over external lines. The Input Cycle Counter becomes permanently enabled and is used to generate the various control signals needed to transmit data from input channel 1 (LEFT) to output channels A and B. and from input channel 2 (RIGHT) to output channels C and D.

Resetting of the counter occurs when a count of 99 is decoded setting the sampling interval to 50 msec. The clock signal running the card is switch to the 2.048 mHz crystal controlled o2/ from the 8080 card. The RD AD/ and WR DA/ commands are generated by decoding states 31 and 63 (decimal) from the Input Cycle Counter. Lastly the output select codes are generated from bit 5 of the Input Cycle Counter.

THEORY OF OPERATION

BLC / SBC BOARD

24May79

DOCUMENT #010-01601

BLC / SBC BOARD

The single board computer specified is a National BLC - 11 or a Intel SBC 10/A. Both have 1k of RAM memory at 3C00 to 3FFF. Both also support four 5 volt 2716 ROM's to provide a total of 8k of ROM at 0 to 1FFF.

NOTE: For product development and test we have a number of BLC - 14's (4k of RAM) and some are equipped with 2708 ROMS. Do not ship these boards.

The following information describes how we set up and use the board - for more detailed information refer to the "BLC 80/11, 12, 14 Board Level Computer Hardware Reference Manual published by National Semiconductor.

The BLC - 11 has 3 parallel ports and one serial port. We configure the serial port to make the computer act as a RS232 data set. During debug and test we configure the "band" rate to 9600 - prior to shipping we will reset the data rate to 300 band, a rate compatable with a large number of terminals and printers.

This port is used to "down load" diagnostics and to provide expanded I/O for diagnostic procedures.

For:	9600 Band	Jumper 4 - 11
	300 Band	Jumper 4 - 8

We will test the 300 rate prior to shipping.

PARALLEL PORTS

We use the "A" port in MODE 2 - that is port A is bi-directional and port C provides control bits for use with port A and control the remote head. Port B is used in MODE 0 - and provides us 4 output bits to the Control Head.

* See Control Head operation for a detailed description. See pg. 4 -35 Hardware Reference Manual for Port description.

The Single Board Computer "SBC" interacts with the 224 High Speed Processor "HSP" through its I/O Bus Multi-Buss.

* See Intel AN-28 for a thorough description of this Buss.

In order to prepare a new board for 224 we have several components to insert and a few jumper changes to make.

The new boards are shipped with the jumpers in default settings - in most instances this is the correct setting for our purposes.

The following table lists all jumper settings organized in numerical order. Those settings which require changing are indicated. All settings should be verified to be on the safe side.

Baud rate setting is called out in a seperate table.

For complete understanding of jumper settings refer to the Hardware Reference Manual.

BLC Jumper List For BLC - 11/14 Using 2716 ROMS in 224 Application

DEFAULT SET AT FACTORY	NON DEFAULT SET BY LEXICON
3 - 4	
13 - 14	67 - 68
15 - 16	70 - 71 FOR 2716
19 - 20	73 - 74
33 - 34	4 - 6 1200/300 BAUD
35 - 36	(4 - 11) 9600 BAUD
44 - 45	EARY PROTOTYPES ONLY
46 - 47	41 - 43 BIDIRECTIONAL PORT
48 - 49	
50 - 51	
54 - 55	
56 - 57	37 - 38 COMMUNICATIONS
61 - 62	2 - 3 RS232
63 - 64	27 - 28 DATA SET
88 - 89	29 - 30
90 - 91	
80 - 81	22 - 23
83 - 84 BLC 11	25 - 26
86 - 87 ONLY	65 - 66
79 - 80	
82 - 83 BLC 14	
85 - 86 ONLY	4 - 11 9600 BAUD

After setting jumpers install 7437's in positions U3 and U6. Install a jumper plug header in U4 with pins 1 - 12 and 4 - 6 jumped.

Install 2716 ROM's in U23, 24, 25 and 26. Always install left to right 23 -> 26. NOTE: That the actual order of installation for 2716 ROMs is Left slot first, then the third slot, second slot and then the fourth slot-eg. [23] [25] [24] [26] The actual ROM's, quantity and contents will be defined in the 224 Software Installation Guide. The actual ROM's installed are determined by the programs purchased by the user. After set up of the SBC it may be tested by installation into a known good 224 and running both diagnostics and actual application programs.

These tests will be added to this document as they become available. TEST PROCEDURE to be appended upon completion of TEST SOFTWARE.

THEORY OF OPERATION

AUDIO INPUT BOARD

7April8Ø

DOCUMENT NO. Ø1Ø-Ø1858

THEORY OF OPERATION - AUDIO INPUT BOARD

The Audio Input Board "A-IN" gain conditions, filters and digitizers two input channels in a floating-point format. The major subsections of the board are:

A. Input Gain Conditioning and Filtering
B. Sample & Hold and Multiplexer
C. Gain Ranger
D. Analog to Digital Converter (ADC)

INPUT GAIN CONDITIONING

Inputs are tranformer coupled and then gain conditioned by a buffer stage with an adjustment range of 15dB. The nominal level at the output of buffer stage U1 is +13dBm (5 volts peak) at 1kHz. This amplitude will just cause limit or full scale of the floating point ADC.

Diode clamps are provided to prevent overloading the input stage of U1.

FILTERS

The input filters are 7 pole active eliptical networks synthesized from FDNR networks. Each pole pair has a trim adjust to compensate for component tolerances. A complete adjustment procedure is described in the test procedure for the Input card.

The nominal cut-off frequency for the input filters is 8kHz to prevent out of band input frequencies from forming alias tones when sampled at 2Ø kHz. The next stage is a shelving pre-emphasis network which provides 2.6dB of boost at 2kHz and 8.15dB at 8kHz. The last filter stage provides aperture correction to compensate the slight amount of high frequency loss introduced by the sample process.

SAMPLE & HOLD AND MULTIPLEXER

The input sample and holds (S & H's) are designed so that when one channel is tracking, the other channel will be in the hold mode. CH1L signal is in the control signal and places U2Ø in the hold mode when high or at logic one this logic one will simultaneously place U21 in the track mode.

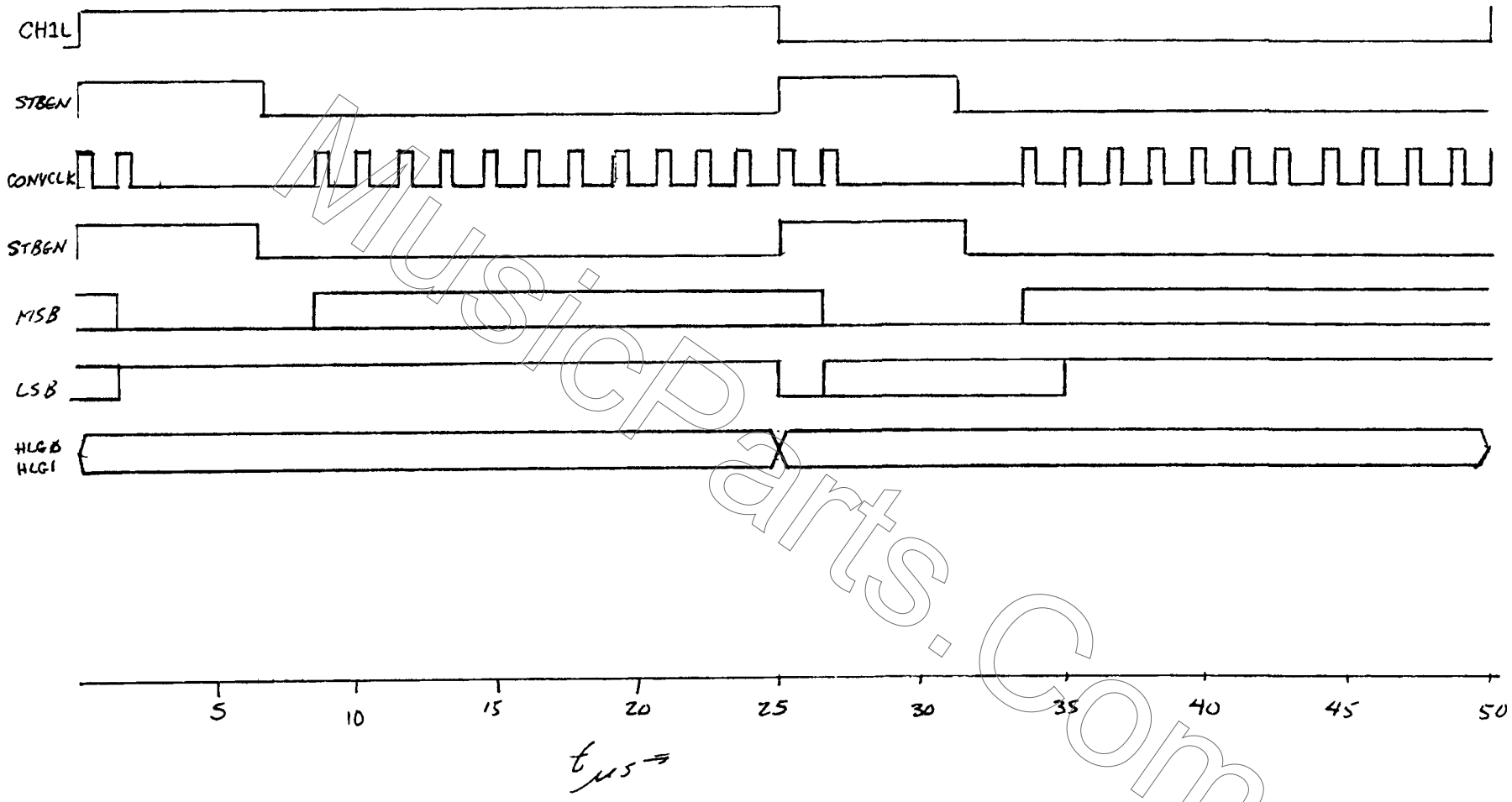


FIG 1 INPUT BOARD TIMING

Analog Switch U22 is controlled by an inverted and level shifted version of CH1L - HLCH1L/. This switch is arranged so that the "held" channel will be commutated to the Gain Switch amplifier (GSA) stage. Figure (1) is a complete timing diagram for this circuit.

GAIN RANGER

Both filtered channels are sent to precision full wave rectifier circuits which give a positive output equal to the peak amplitude of their inputs. The tracked channel rectified output is routed by Analog switch U14 to an amplitude quantizer made up of 5 comparators biased at 5.0V, 2.24V, 1.12V, 0.56V, and 0.280 Volts. These thresholds are arranged so that 5 Volts corresponds to limit for the ADC and that each of the lower thresholds are 6dB apart and allow determination of the optimum gain to be used for the GSA. The following table of comparator outputs show how the proper gain is selected for various amplitude signals.

SIGNAL	U15-13 (5.0V)	U15-1 (2.2V)	U15-2 1.12V	U16-1 560MV	U16-2 280MV	GAIN A	IGA1	IGA
>5.0V	0	0	0	0	0	0dB	0	0
2.24-5.0	1	0	0	0	0	0dB	0	0
1.12-2.24	1	1	0	0	0	6dB	0	1
560mV-1.12V	1	1	1	0	0	12dB	1	0
280mV-560mV	1	1	1	1	0	18dB	1	1
<280mV	1	1	1	1	1	18dB	1	1

The above comparator outputs are decoded and latched to provide gain control signals IGA0 and IGA1.

The 5 Volt and the 280MV comparator outputs are needed for headroom display purposes only while all of the additional comparators provide gain change information and headroom display. Note that the gains are arranged so that 6dB of gain is added whenever a signal falls below 45% of full scale. A signal approaching 45% of full scale would then be increased by a factor of two to about 90% of full scale so as to better take advantage of the ADC's useful dynamic range. It is probably worth calling attention to the fact that the actual technique of gain ranging used here is commonly referred to as instantaneous floating point coversion - that is, an appropriate gain is selected immediately prior to converting each sample. The gain thus follows the envelope of the converted signal.

It can be demonstrated that good signal reconstruction can be achieved provided that the ADC is properly offset so as to deliver a zero code for Ø Volts input.

Good gain match is provided by using a precision resistor network to set the gain of U23. The resistor feedback ratio is selected by Analog switch U24.

Since U24 conducts negligable current, errors due to switch resistance are negligable. U24 also provides a decode function for the gain bits HLGØ and HLG1. It can be shown that voltage offset in this stage is not important provided that it is proportional to gain.

Maximum offset due to accumulated errors should never exceed 8ØMV at this stage output.

ANALOG TO DIGITAL CONVERTER

The Analog to Digital Converter (ADC) is a successive approximation type. A 12 bit current output DAC is sequenced by a SAR chip U26. This device receives its start command and conversion clock (STCONV) and (CNVCLK) from the FPC card. An LM211 comparator is used to compare the DAC's output with the input signal - the output of this comparator is used as the data input to the SAR. Refer to the timing diagram for details of this circuits operation.

THEORY OF OPERATION

AUDIO OUTPUT BOARD

7April80

DOCUMENT NO. 010-01857

THEORY OF OPERATION - AUDIO OUTPUT BOARD

The Audio Output Board provides 4 output channels serviced from a single time shared DAC and Gain Switch Amplifier.

The DAC U2 is updated with a 12 bit word DA0 - DA11. The DAC responds with an analog output in the range of -5 to +5 Volts. Gain control is set by two bits OGA1 and OGA0 which program analog switch U3. U3 selects one of 4 taps from a precision divider network RD2. Gain selection is either 1, 1/2, 1/4, or 1/8 +/-0.05%. U4 operates as a high input impedance follower to prevent loading of the attenuator network.

Channel selection signal OUTA, B, C or D becomes high 2.93us after DAC and Gain data becomes valid. This delay allows time for the DAC and GSA to settle prior to placing the selected output sample and hold in the sample mode. The OUT (sample) command is valid for 6.8us. During this time U6 switches the output gain conditioned DAC voltage to capacitor C13, 16, 17 or 20. U7 and U8 provide high impedance buffering to prevent discharge of the sample capacitors during the hold period.

The +7 and -7 Volt CMOS switch bias is provided by Zener regulators CR5 and CR6. Power-on muting function is provided by transistor Q9 which is held in cut-off for several seconds after power is applied. R159 charges a 22uf capacitor from -7 Volts towards +7 Volts. Saturation of Q9 places a ground signal on pin 6 of U3 thus enabling it to pass signal.

Output de-emphasis is provided by stages U13 and U21. Filtering is provided by 7 pole Cauer (elliptical) filters. Adjustments to compensate component sensitivity are provided for each section. These settings should never need adjustment provided related components are not changed. Should adjustment be required the following procedure is given. The same procedure is applicable for each section.

A. Inject 11.815 kHz at 0.5 Volt peak into R43 high side. Adjust R19 for a null at the R20, 26 node.

B. Inject 10.24 kHz at 0.5 Volt peak into the R20, 21 node. Adjust R25 for a null at the R26, 27 node.

C. Inject 19.12 kHz into the R26, 27 node. Adjust R31 for a null at the R32, 33 node.

The output stage consists of a level adjustment potentiometer and an op-amp stage with complementary output transistor buffers. Overall, negative feedback is provided around the stage to maintain fixed gain and provide low distortion. A loading network is also provided to maintain high frequency stability.

Each output stage drives an output transformer on the Chassis transformer card. The output transformer provides a voltage gain of about 2.5.

THEORY OF OPERATION

REMOTE CONTROL HEAD

24May79

DOCUMENT NO. 010-01600

THEORY OF OPERATION - REMOTE CONTROL HEAD

INTRODUCTION

The Remote Control Head consists of two board assemblies joined by a 27 conductor flexible cable.

The display and push button board has no electronics other than 3 diodes, 8 current limiting resistors, switches and LED displays. The second board contains all the electronics, slidepots and a 25 pin I/O connector. The I/O connector contains 14 signal wires and 2 power wires - the remainder of the 25 lines are used for digital and chassis ground returns. Ground returns are placed between signal lines which could interfere with each other. This technique together with the power delivery scheme allow use of reasonably long ribbon cables with good results.

The Remote Head interfaces to the BLC/SBC board level computer through a 25 pin cable then makes a transition at the mainframe to a 50 conductor cable which in turn connects to the J1 edge connector of the SBC/BLC board.

The transition from 25 to 50 conductors is made at a small board called a Transition Board. The Transition Board is also used as a point to inject a 10 Volt RMS AC power source from a seperate secondary of the power transformer. The 10V is fused on the Transition Board to protect against cable shorts or similar fault conditions.

Table 1 lists all the cable runs and tie points between the Control Head and the SBC/BLC Computer Board.

TABLE 1
REMOTE HEAD WIRE LIST

25 Connectors/Panel to Mainframe Cable	50 Pin Cable, Xsistion Connector/SBC/BLC Edge Conn.	Function Name
1	2	GND
2	1	PB3
3	3	PB2
4	5	PB1
5	7	PB0
6	4, 6, 8	GND
7	* TO CHASSIS	CHASSIS GND
8	20	GND
9	21, 29	PC1
10	30	GND
11	25	PC0
12	26	GND
13	33	PA7
14	35	PA6
15	37	PA5
16	39	PA4
17	47	PA3
18	45	PA2
19	41	PA1
20	43	PA0
21	34,36,38,40,42,44,46,48	GND
22	* TO 10 VOLT	AC1
23	SECONDARY	AC1
24	* TO 10 VOLT	AC2
25	SECONDARY	AC2

* NOT CONNECTED TO SBC/BLC BOARD

THEORY OF OPERATION

POWER SUPPLY

DISPLAY SCAN

SLIDE POT DIGITIZATION

SWITCH DATA

POWER SUPPLY

The power supply consists of a full wave bridge with filter and a 5 Volt 7805 regulator. The unregulated DC is used to directly supply the LED displays.

The reason for rectification at the control head is to allow transmission of power through the control head without suffering IR voltage drop in the ground returns. Voltage drop in the ground returns would degrade noise margins and add LED noise spikes to the logic signals. Figure 1 indicates the various current paths and demonstrates this concept of an isolated control head power source.

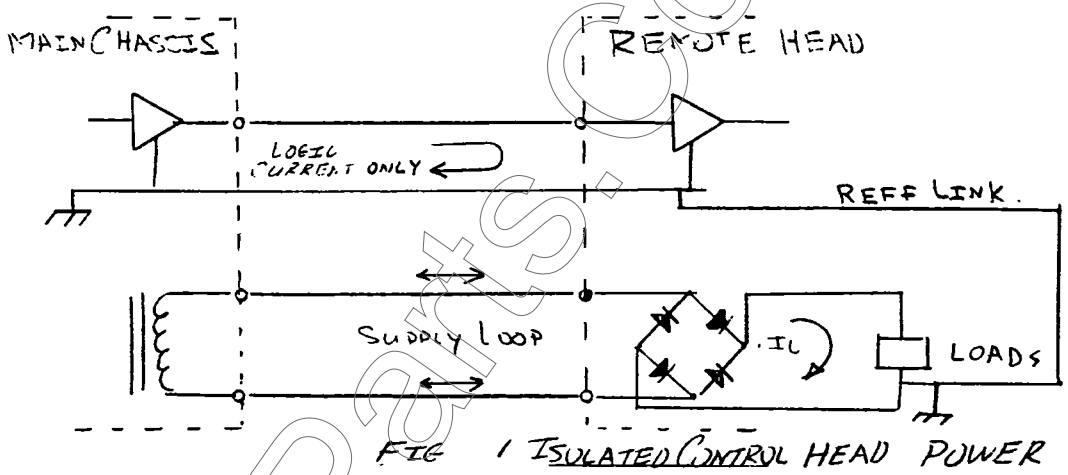


FIG 1 ISOLATED CONTROL HEAD POWER

DISPLAY SCAN

The display section is based on a scanned display concept in which all digits share a common segment drive. All digits are common cathode and current will flow through digit segments only if the cathode for that digit is grounded. The display and data transfer section of the Remote Head were designed to use as few as possible interconnection wires. All segment data goes out on 8 lines from Port A and a 4 bit digit address goes out on Port B. Port C sends out control signals to begin display and to start data conversion. (digitize pots).

The display cycle in controlled by software and at the end of this cycle the 8 Port A lines are used to send Pot or Switch data back to the computer. The address for the switches and pots would be the same as that just used for a digit during a display cycle.

The following table lists the various display and read back device addresses. The commands sequence used would be as follows:

ACTION

Load Digit, Port B
Load Segments, Port A
Sets PC2/, ACK/
Sets PC0 (ST Conv)
Clears PC0
  .
 Delay Approx. 500us
  .
Clears PC2/
Sets PC1/, Read Enable
  .
Delay 12us
Reads Data
Clears PC1/
  .
  .
Select Next Digit
Repeat Sequence

Digit select is implemented by a 74LS42 4 to 10 line decoder. The digit selects are used to control 75376 high current drivers.

The LED's are arranged into 8 digits. Digits 0, 1 and 2 are the 3 seven segment displays while digits 3 through 7 are groupings of the various discrete LED's on the panel. Refer to the schematic for details.

The segment drive is provided by 75327 dirver arrays current limited with 150 ohm resistors. Function RDENB is used to disable segment drive when the 8 data lines are used for transmission of POT or SWITCH data.

Each time a display cycle is started, one shot U2 is fired to enable the 75326 drivers for a period of several ms. In the event that the computer hangs the one shot will time out and shut down all displays to prevent sustained high current (50ma) from being drawn by any LED. It should be noted that the LED's are run at high current for a brief period of time. Since the average duty cycle is low the LED's will not over heat.

The preceived brightness level is enchanced by the high peaks even though the average current is quite low.

SLIDE POT DIGITIZATION

The ADC-0817 is a complete A/D subsystem capable of scanning up to 16 inputs and converting each input amplitude representation to an 8 bit binary code. The only inputs are clock, a start convert pulse and address.

The ADC-0817 is used in a ratiometric configuration - that is the pot high terminals and chip +REF. are tied to 5 volts and the low terminals and ground (0V) are tied to the -REF. The pots are noiw presenting the complete range from REF to +REF to the ADC as a linear function of Slide Position. The ADC translates this to 00000000-11111111 codes.

The start convert pulse (STCONV) is filtered for noise rejection and presented to the start-convert and address latch inputs of the ADC. The ADC will sychronize this command to its free running input clock and begin a conversion cycle. Within ~ 64 clock cycles or 128us assuming a 500kHz clock, the 0817 completes the conversion and presents its data to tri-state outputs which are hand-wired on. Selection of the desired pot is done by an internal analog multiplexer.

This device (ADC 0817) is a cmos circuit and should be treated so as to prevent static damage.

The clock is produced by a cmos/RC free-running square wave oscillator running at a nominal 500kHz +/- 150kHz (+/-30%). The actual conversion time will range from 70-130us. Frequency should be verified during pre-test. Data from the 0817 outputs is gated onto

the PA0-7 data bus when REDENB/ is low and the digit address is 0 through 5. A tri-state LS244 is used for this function. Figure 3 shows typical waveforms for the ADC-0817.

SWITCH DATA

The switches are all N.O. push buttons arranged in 3 bank corresponding to DIGITS 6 through 8.

Germanium diodes 1N283 are used to isolate each bank or column of switches in the event that more than one button is pressed at the same time.

The banks are wired into rows assigned to the PA 0-8 data lines. Pull up resistors are provided to insure proper thresholding for the 224 tri-state buffers.

A complete bank or column of switches can be read when RDENB/ is low and the bands digit line is selected.

Any pushed button will be put on the bus as a TTL low or a logic "1" as interpreted by the SMP/BLC computer.

Refer to the schematic or Table 1 for details of button and pot assignments.

TEST AND CALIBRATION

24May79

T & C CALIBRATION PROCEDURE

1. Connect Channel A scope to Pin 3 of U58 (sync. on A)

2. Connect Channel B to Pin 2 of U59 - (Clip on the end of R2, 1K, Resistor).

3. Adjust C32 for a loop control voltage of between 3.6 and 4.0 volts (3.8 exactly is preferred) (actual voltage depends on jitter being reduced).

4. Verify absence of lock up by grounding Pin 3 of U53 and then removing ground. Loop should return to proper operation immediately.

5. Compare Pin 1 and Pin 3 of U58 to determine jitter - should be 10ns or less. MCE can also be compared to Pin 1 of U53.

24May79
DOCUMENT NO. 010-01603

ANALOG INPUT TEST PROCEDURE

1. EQUIPMENT REQUIRED

1. 224 Frame with FPC and Analog Output Board - (an SBC Board or 2MHZ clock will also be required).
2. Signal Generator - KHRON-HITE MODEL 4300A or similiar.
3. Scope - DC - 25MHz 2 channel.
4. Counter
5. DVM
6. Cables, Dip Clips and Probes.
7. Noise and THD Measuring set up HP 331.

PROCEDURES

1. Set up mainframe with board under test (BUT) on an extender card. Power up and measure +/- 7V supplies at test points. These voltages should measure 7 volts +/- .7V or 6.3 to 7.7 volts. Test points are next to input gain pots. Next check for hot IC's or any other abnormal condition. (Smoke is abnormal)
2. Inject signal (use a T connector to both input channels). Set OSC to 1kHz and +12dBm output. This 1kHz @ +12dBm source will be referred to as a standard input.

NOTE: Steps 3,5,6,10,13-18 must be performed on all boards. These steps have an * before the step no.

*3. GO FOR BROKE

This procedure will allow you to test for overall card operation prior to detailed operation. If it passes this test we call it a PDGB (Pretty Damn Good Board). If it does not pass, the following procedures will narrow down the problem. In either event certain performance and calibration tests will still have to be done.

Check for audio output on channels A, B, C, and D. Adjust Input Gains R1 and R2 for an output level of +12dBm (just below limit). Outputs A and B will be from the LEFT. Input and Outputs C and D will be from the RIGHT input.

For abnormal or missing outputs try to record the symptoms for latter reference to help you narrow down problems.

4. TEST AND CALIBRATION

Test and Calibration - STD Input

Adjust Input Gains R1 and R2 for +/-5V swing at U1 pin 1 and pin 7. Verify a clean undistorted +/-5V signal at U6 pin 7 and U11 pin 7.

If signal at U6 and U11 pin 7 is not proper, do a stage by stage check to determine the problem before proceeding.

*5. FILTER CALIBRATION

This procedure can either be performed using a 3 frequency calibration oscillator or a standard oscillator with a frequency counter attached to insure accurate setting. Use an amplitude of +/-Ø.5V peak.

A. Inject 11.815kHz at the input of U1 (Refer to schematic 060-01321). Monitor signal at node of R13, R15 (R40, 42,channel 2). Adjust R19 (R46 for channel 2) for a null at the measurement point.
B. Inject 10.240kHz @ Ø.5V peak at R13, R15 node (R40, 42 for channel 2). Adjust R25 (R57 for channel 2) for a null at the node of R14, R21 (R41, 48 for channel 2).
C. Inject 19.120kHz @ Ø.5V peak at R14, R21 node (R41, R48 for channel 2). Adjust R31, R57 for a null at R20, R27 node (R47, R54 for channel 2).

If any nulls can't be obtained, carefully examine all component values associated with stage in question.

Place a dot of green lacquer on each calibrated pot to prevent future tampering.

*6. FILTER BANDPASS

Input 1kHz at ØdBm to both channels. Monitor filter output at U5 pin 6 (U10 pin 6 for channel 2). Sweep the oscillator through the range of 100Hz to 10kHz, observe frequency response. Refer to Fig (1A) for a correct response. Investigate any deviations from this plot greater than Ø.5dB.

7. COMPLETE INPUT RESPONSE

Monitor U6 pin 7 (U11 pin 7 for channel 2). Compare this response to Fig.(1B) - investigate any deviations greater than Ø.5dB.

8. VERIFY OPERATION

Verify operations of full wave rectifier circuits and functioning of Analog switch by probing U14 pin 15. Compare to Fig. (2).

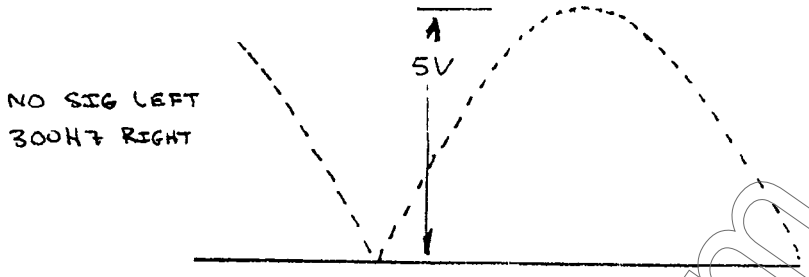


FIG 2

FULL WAVE RECTIFIER

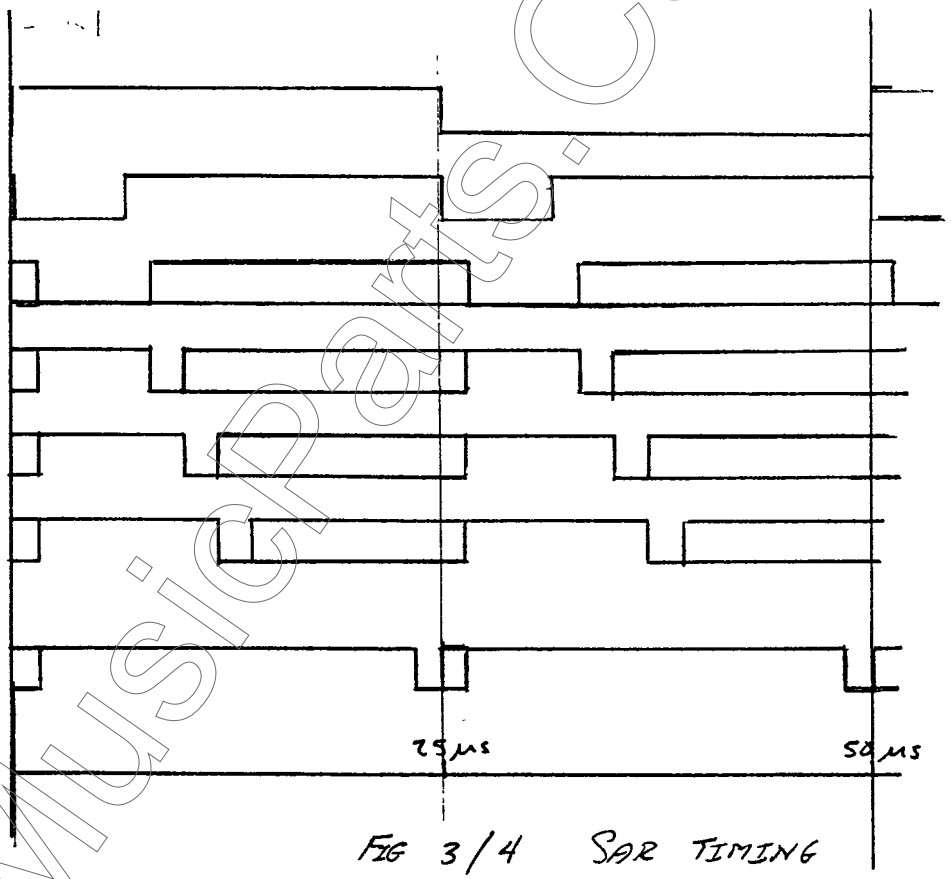


FIG 3/4 SAR TIMING

9. VERIFY THRESHOLD POINTS OF COMPARATORS

Verify threshold points of comparators U15 and U16 - all voltages should be ratioed within 1% and accurate to with +/-2% on an absolute basis.

The following table list's the voltage limits for this test point.

NOMINAL 5V - 4.9 to 5.1V
NOMINAL 2.24V - 2.20 to 2.28
NOMINAL 1.12V - 1.10 to 1.14
NOMINAL .560V - 0.549 to 0.571
NOMINAL .280V - 0.274 to 0.286V

*10. VERIFY HEADROOM DISPLAY - (If full 224 Chassis available)

GENERATOR LEVEL	-24	-18	-12	-6	0
+12dBm	x	x	x	x	x
+11dBm	x	x	x	x	0
+5dBm	x	x	x	0	0
-1dBm	x	x	0	0	0
-7dBm	x	0	0	0	0
-13dBm	0	0	0	0	0

X = ON
O = OFF

11. GSA OPERATION

Input a 100Hz +12dBm signal to both channels. Sync. scope from generator output. Observe waveform at U23 pin 6. Gradually lower input and observe action of Gain Ranging. Compare this operation to a known good board.

12. ANALOG TO DIGITAL CONVERSION

Sync. scope on CHIL and observe STCONV pulse and CNVCLK signals. Compare to Fig. (3). Use a 1kHz standard input and observe each SAR output at U26 in the following order 21, 20, 19, 18, 17, 16, 9, 8, 7, 6, 5, 4. Compare to Fig. (4). Check for stuck or shorted bit lines.

If operation is inproper, check U27 comparator operation.

*13. OFFSET CALIBRATION

Assuming that the Input Analog Board is working correctly a single offset calibration is now required. (Mainframe +/-15V must be 15+/-100MV). Power down and carefully remove U23 connect jumper from U23 socket pin 6 (hook onto CR21 cathode) and connect the other end of the jumper to a quiet ground, C73 low side. Power up and connect one scope channel to U19 pin 1 (CHIL) and the second scope channel to U26 pin 21 (MSB). Sync. the scope on CHIL (positive going) and set scope to 5us / DIV. and 2V / DIV. on each channel. Offset (R90) should now be adjusted so that the MSB dithers between 1 and 0 with equal intensity when viewed on the scope.

See Fig. (5)

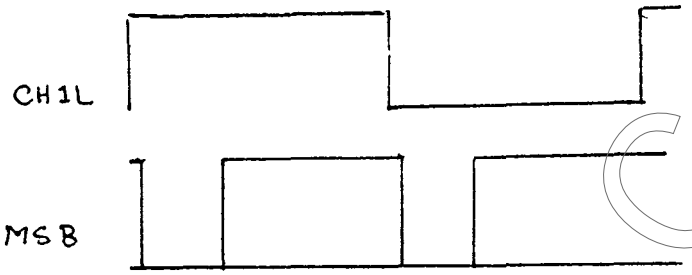


FIG 5. OFFSET ADJUST OF MSB.

Place a dot of green lacquer on R90 and power down and replace U23. The above procedure insures that the ADC responds with code 100000000000 or 011111111111 for a true 0 volt input. This will insure good gain step matching during output conversion.

*14. GSA OFFSET

With both inputs terminated with 600 ohms, measure offset at pin 6 of U23. Sync. scope on CHIL and use a unity gain probe to measure offset. Max offset for channel 1 or channel 2 should be less than 80MV.

*15. CHANNEL SEPARATION

Insert standard input into both channels. All outputs should read +12dBm out. Remove the left input 600 ohms termination and measure output C and D - output should be at least 60dB below limit or less than -48dBm. Repeat for outputs A and B while inputing to LEFT channel - terminate RIGHT input. Output should again be -48dBm or less U22 performance greatly influences channel seperation.

*16. THD AND NOISE

THD and noise at 1kHz and 8kHz should be measured for both LEFT and RIGHT channels.
at +12dBm and 1kHz THD and noise should be less than .Ø5%
at ØdBm in and 8kHz THD and noise should be less than Ø.5%.

*17. NOISE

With inputs terminated and with a known good output card both LEFT and RIGHT channels should have an output noise reading as per the following:

	WIDE BAND 2Ø -2ØkHz	A WEIGHTED
absolute	<-58dBm	<-8ØdBm
rel to +12dBm	8ØdB S:N	92dB S:N

*18. INPUT SENSITIVITY

Adjust generator output for +8dBm. Advance input gain adjust pot until limit is reached - the gain pot should be close to its full clockwise rotation. Next set generator for +18dBm and rotate input gain pot CCW until the unit just comes out of limit. This should be close to full CCW rotation.

Design tolerances allow most machines to operate with a +7dBm to +22dBm input range - however the spec is +8 to +18dBm.

24May79

Document #010-01604

ANALOG OUTPUT TEST PROCEDURE

1. EQUIPMENT REQUIRED

1. Known good 224 Mainframe with SBC, FPC and Analog Input Cards.
2. Scope
3. Test Oscillator - KHRON-HITE 4300 or similar. * Three frequency Oscillator for filter calibration is optional
4. THD and Noise measuring test set - HP 331 or similar.
5. Frequency Counter
6. Noise Meter
7. Extender Card
8. 600 ohm load

PROCEDURE

Install board on extender card and power up 224 in self-test mode. Check for overheating components or any other signs of abnormal behavior.

1. Test (measure) +/-7V supplies - correct range would be 6.3 to 7.7 volts.
2. Set generator for +12dBm @ 1kHz (standard input). Check each output channel for output audio.
3. Verify that each output can deliver +8 to 18dBm output into a 600 ohm load after performing this test on each output set each output gain for +12dBm exactly.

NOTE: Each output stage has a test point on the high side of it's attenuator pot. These test points should give +5 volts output at 100Hz when the input ADC is just at the "limit" point. Limit can easily be seen when the waveforms begin to flat-top. This action is very obvious even for higher frequency signals if the sample and hold outputs are examined (U7 and U8 pins 1 and 7).

4. CALIBRATE FILTERS

Each of the four output filters have 3 null adjustments to compensate component sensitivity. The procedure outlined below for channel "A" should be done for all four channels.

A. Inject 11.815kHz at 0.5V peak at R43 high side. Adjust R19 for a null at the R26, R276 node.
B. Inject 10.24kHz @ .5V peak into the R20, R21 node and adjust R25 for a null at the R26, R27 node.
C. Inject 19.12kHz into the R26, R27 node and adjust R31

for a null at the R32, R33 node.

If nulls can't be obtained, carefully examine all component values of the stage in question.

D. Repeat for channels B, C, and D. Refer to schematic for corresponding test points

5. OUTPUT FREQUENCY RESPONSE

Verify system frequency response for each channel against Fig. 1

6. THD, NOISE AND OFFSET ADJUST

THD and Noise to be measured at 1kHz and 8.0kHz.

+12dBm	IN	1kHz	< .05% max
		8kHz	< .5% max
0dBm IN			

7. CHANNEL SEPARATION

Remove LEFT channel input and terminate input. Provide STD input to RIGHT channel. Residual signal measured in channel A and B should be 60dB below +12dBm or -48dBm max.

Remove RIGHT channel input and terminate. Restore input to LEFT channel. Again residual in channel C and D should be less than -48dBm.

8. POWER OR DELAY

Check operation of power on delay circuit (Q9). Audio output should enable within 2 to 3 seconds of power up.

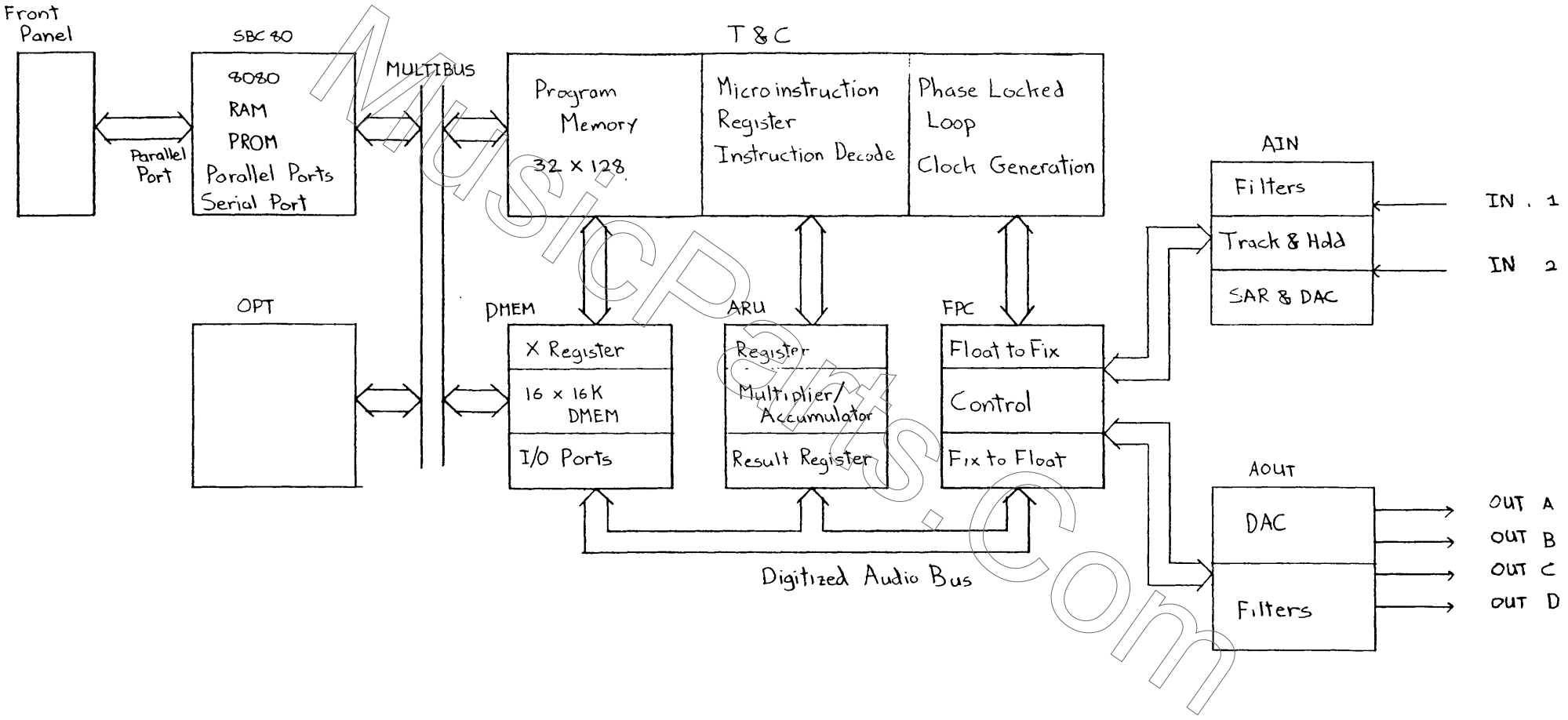


Figure 1.1
Model 224 Block Diagram

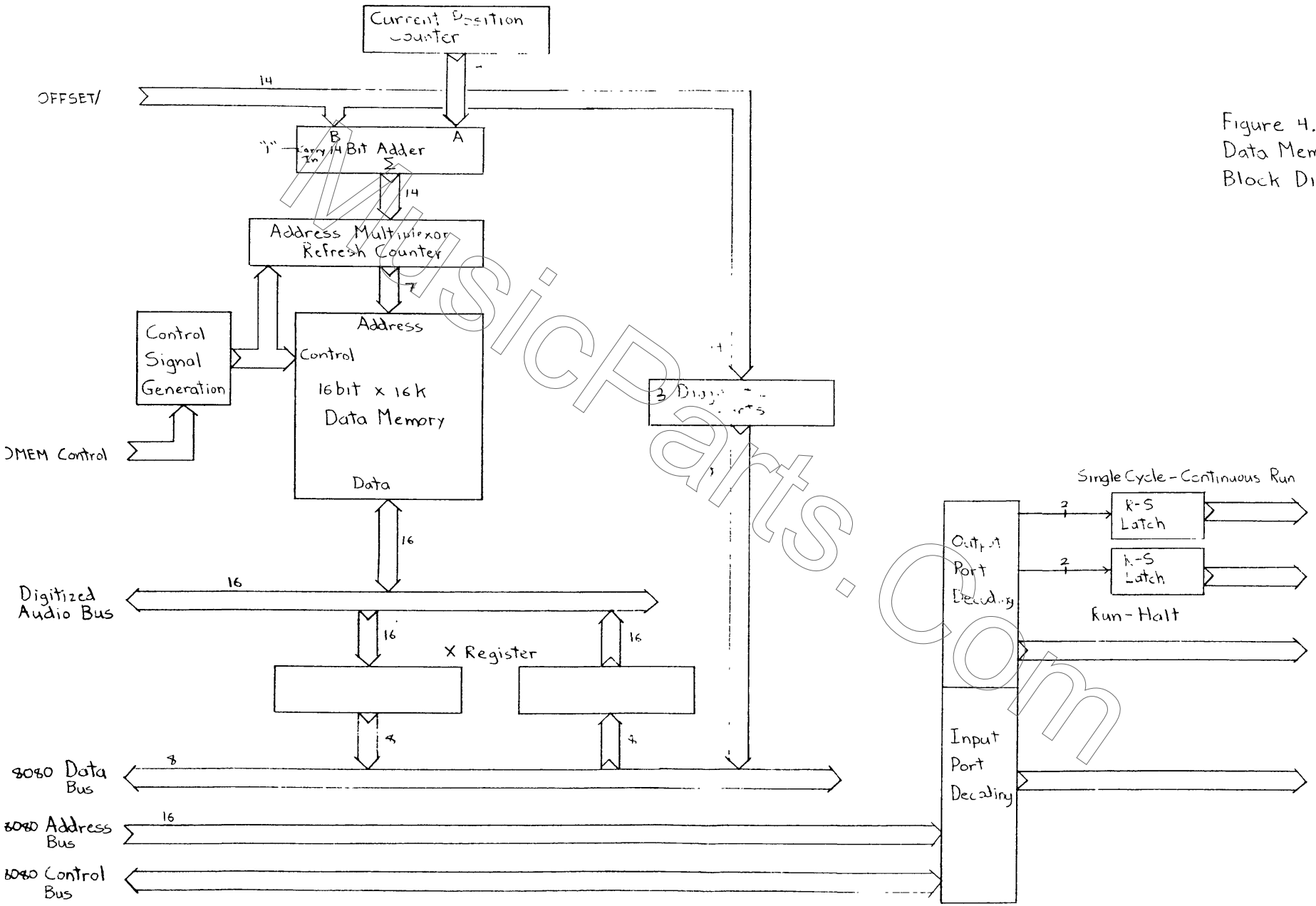


Figure 4.1
Data Memory Card
Block Diagram

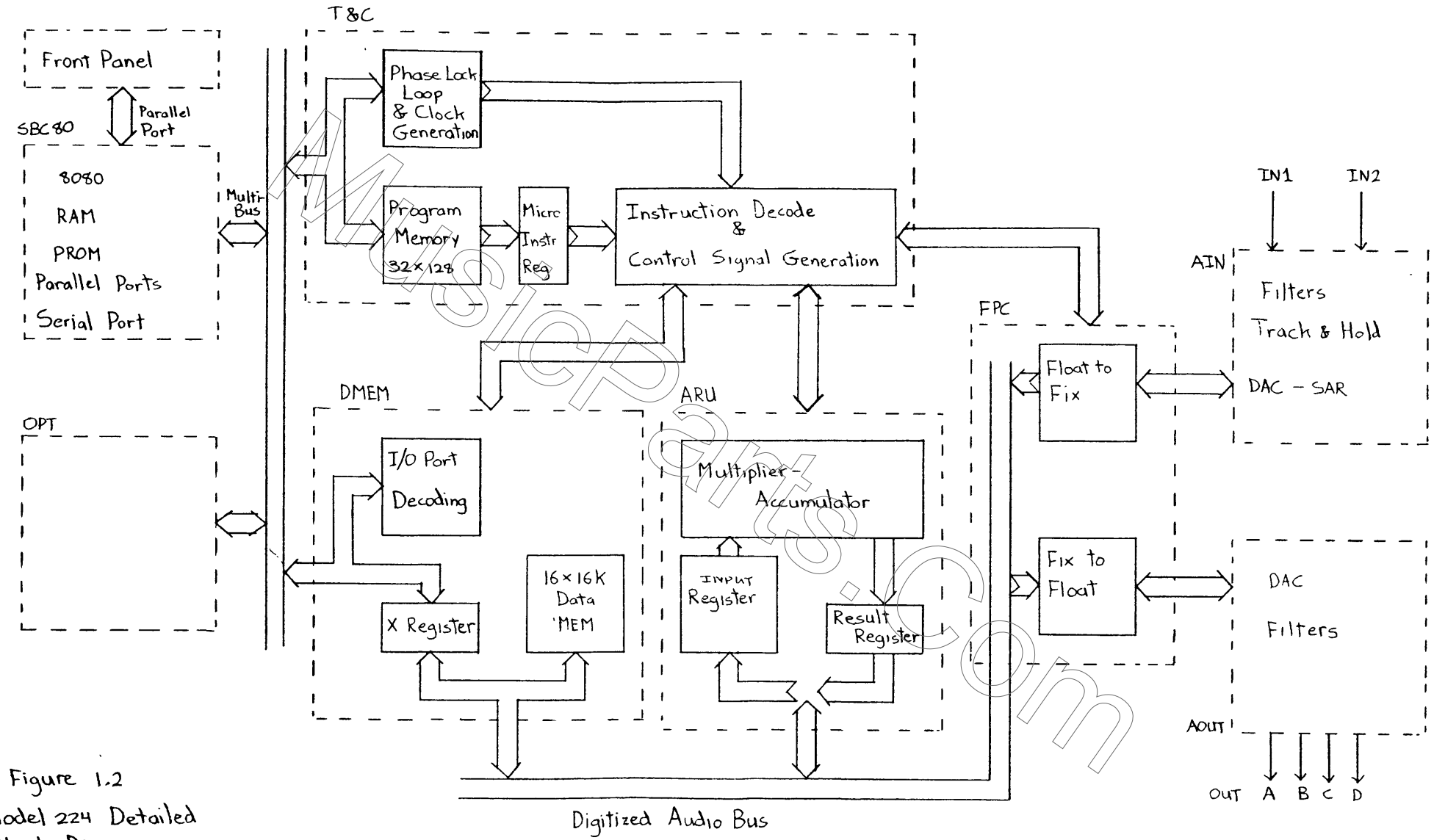
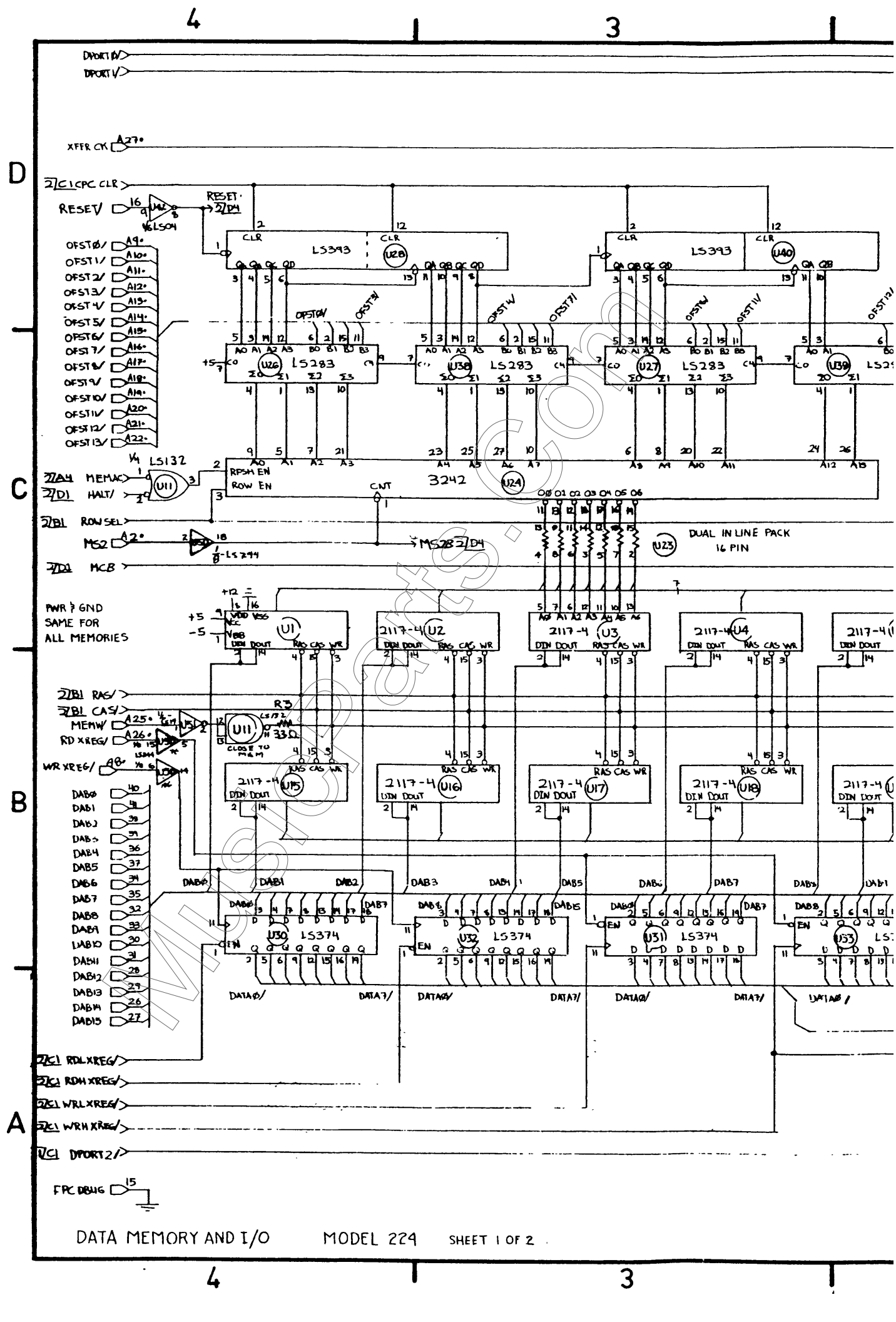
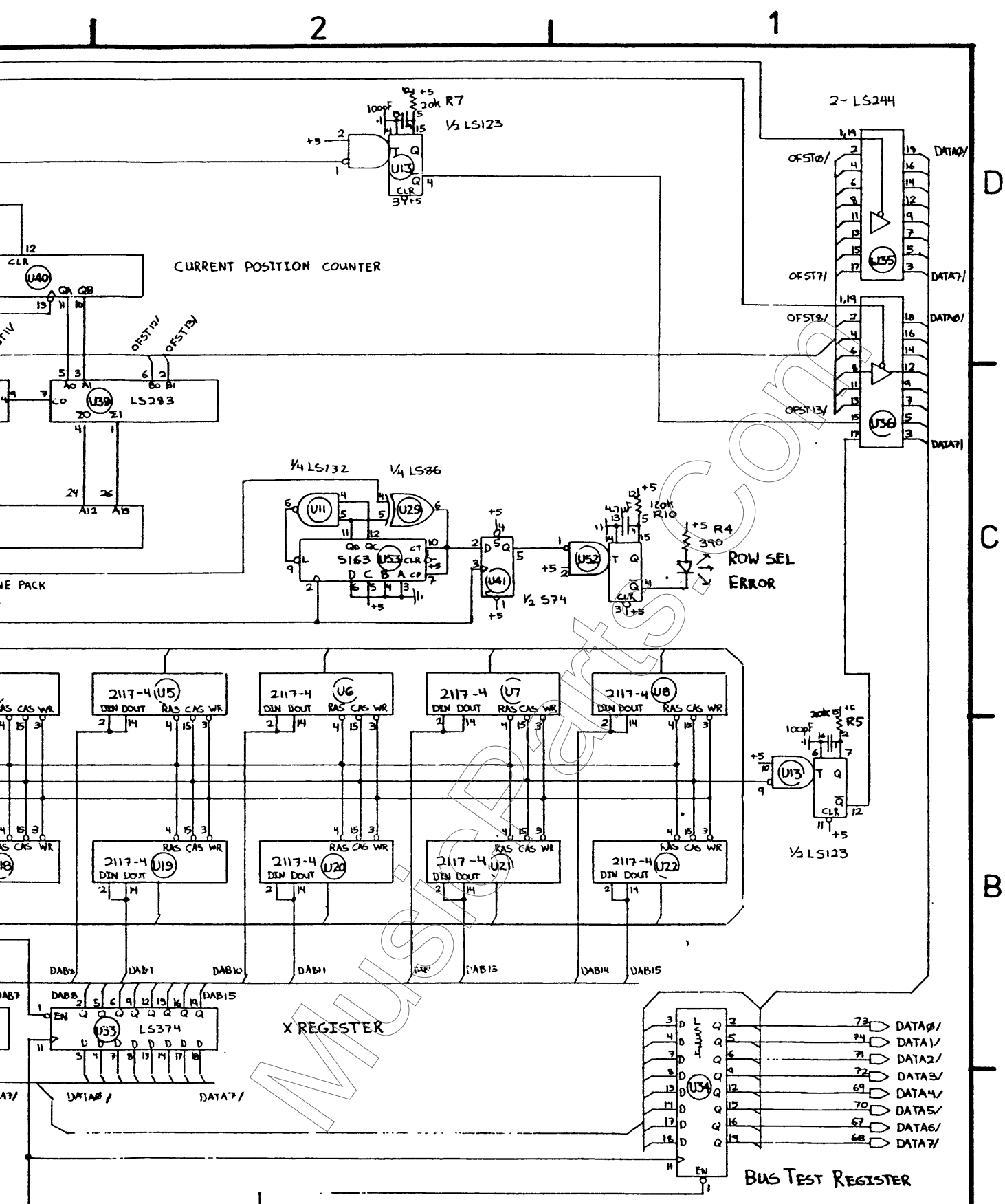


Figure 1.2
Model 224 Detailed
Block Diagram


DPORT 0/
DPORT 1/
XFER CK
A27
RESET/
RESET
2/D4
2/C1 CPC CLR
OFST0/
OFST1/
OFST2/
OFST3/
OFST4/
OFST5/
OFST6/
OFST7/
OFST8/
OFST9/
OFST10/
OFST11/
OFST12/
OFST13/
LS393
LS283
3242
2/A4 MEMAC
2/D1 HALT/
2/B1 ROW SEL
MS2
MCB
LS132
LS74
MS2 2/D4
CNT
DUAL IN LINE PACK
16 PIN
PWR & GND
SAME FOR
ALL MEMORIES
2117-4
RAS CAS WR
DIN DOUT
2/B1 RAS/
2/B1 CAS/
MEMW/
RD XREG/
WR XREG/
33Ω
CLOSE TO M & M
DAB0
DAB1
DAB2
DAB3
DAB4
DAB5
DAB6
DAB7
DAB8
DAB9
DAB10
DAB11
DAB12
DAB13
DAB14
DAB15
LS374
DATA0/
DATA7/
2/C1 RDL XREG/
2/C1 RDH XREG/
2/C1 WRL XREG/
2/C1 WRH XREG/
2/C1 DPORT 2/
FPC DBUG
DATA MEMORY AND I/O
MODEL 229
SHEET 1 OF 2



11/30/79 R9, R10 WERE 200K; NOW 120K.
11/7/78 ADD 1 to 47,A9

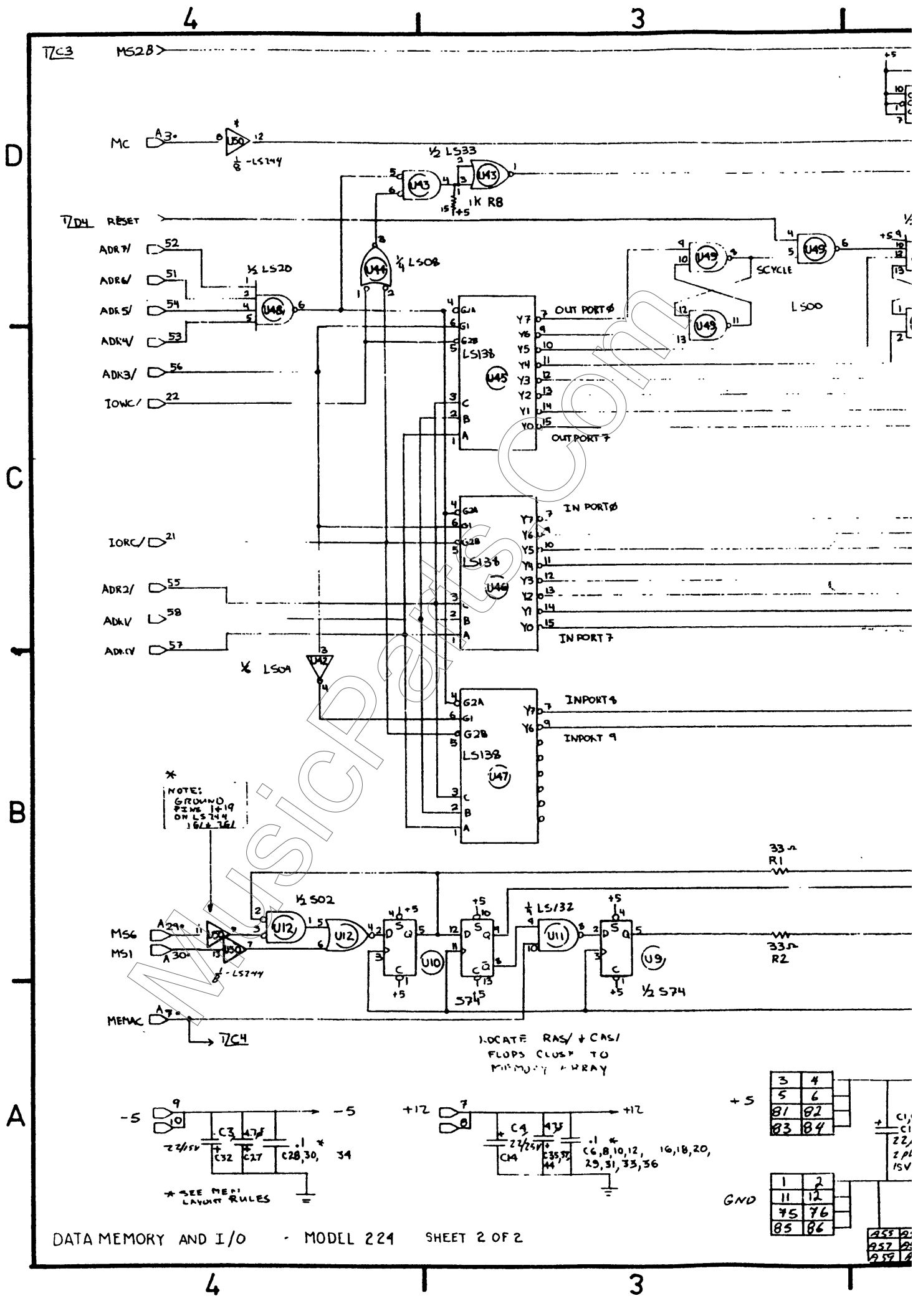
LEXICON INC, WALTHAM MA 02154

SCALE NA	APPROVED BY CB 7-26-79	DRAWN BY R. KAO
DATE 7-12-78		REVISED 11/30/79

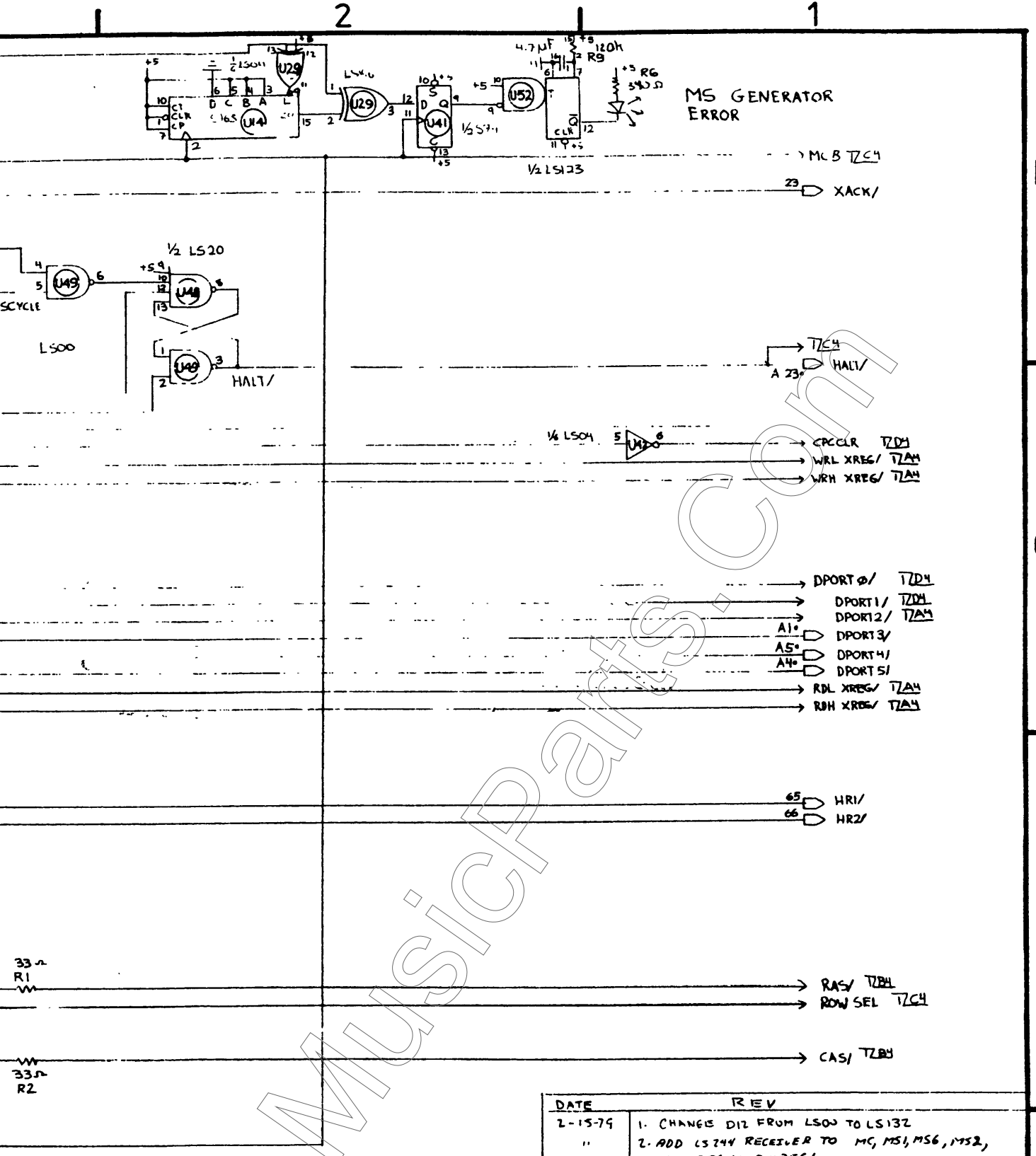
DATA MEMORY AND I/O - MODEL 224

SHEET 1 OF 2

DRAWING NUMBER 060-01319



DATA MEMORY AND I/O - MODEL 224 SHEET 2 OF 2



DATE	REV
2-15-79	1. CHANGE D12 FROM LS00 TO LS132
"	2. ADD LS244 RECEIVER TO MC, MS1, MS6, MS2, RDXREG, WR XREG/
"	3. ADD LS14 to RECEIVE MEMW/
"	4. USE SPARE SECTION OF C13 FOR INVERTER
"	5. USE D12 FOR SECOND INVERSION OF MEMW
3-16-79	6. ADD ADDITIONAL GROUND PINS — A55 — A60 ADDED COMPONENT DESIGNATIONS FOR PC BOARD LAY

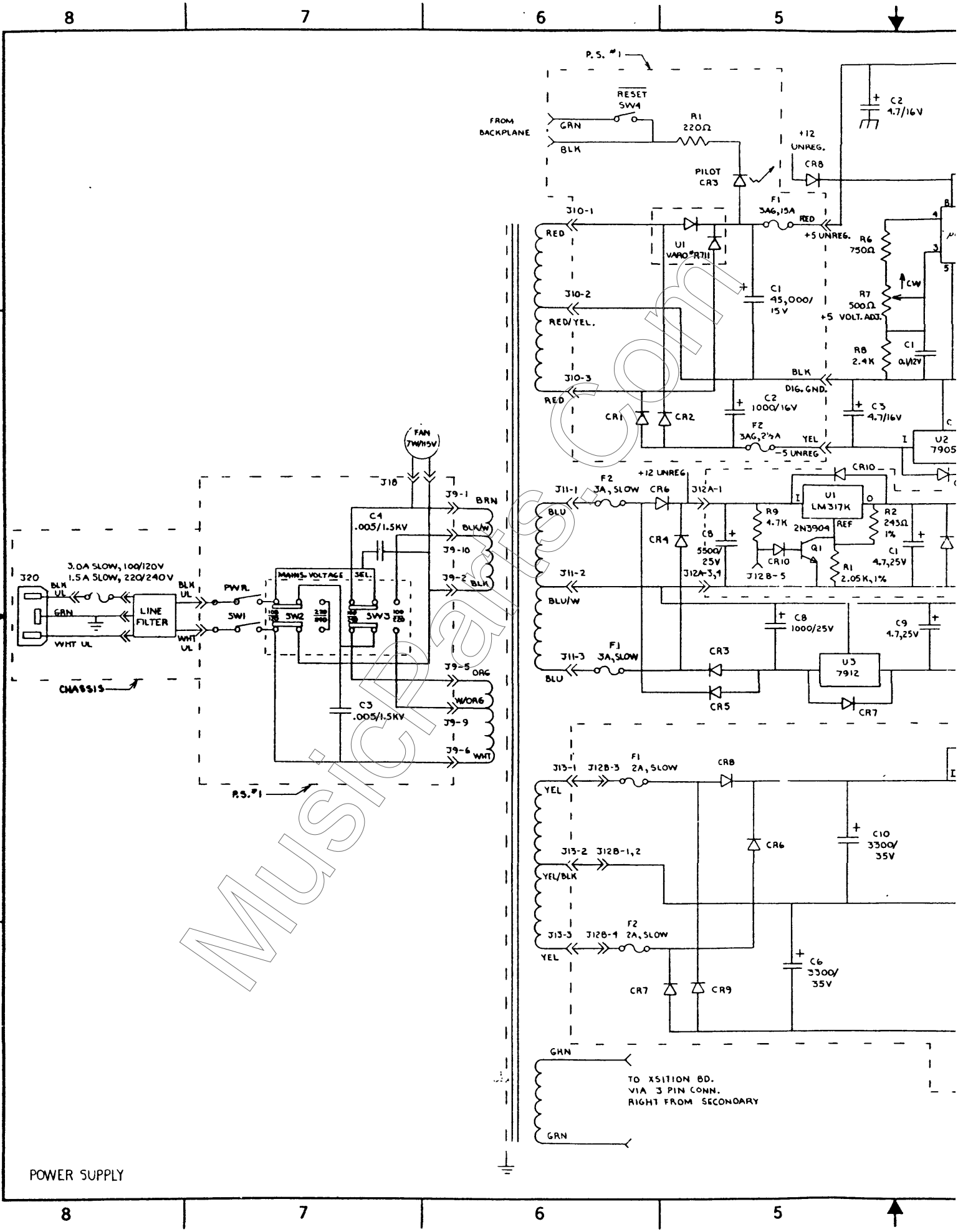
EXICON INC, WALTHAM MA 02154

SCALE	APPROVED BY	DRAWN BY
NA	CB 7-26-79	R. KAO
DATE 7-12-78		REVISED 11/30/79

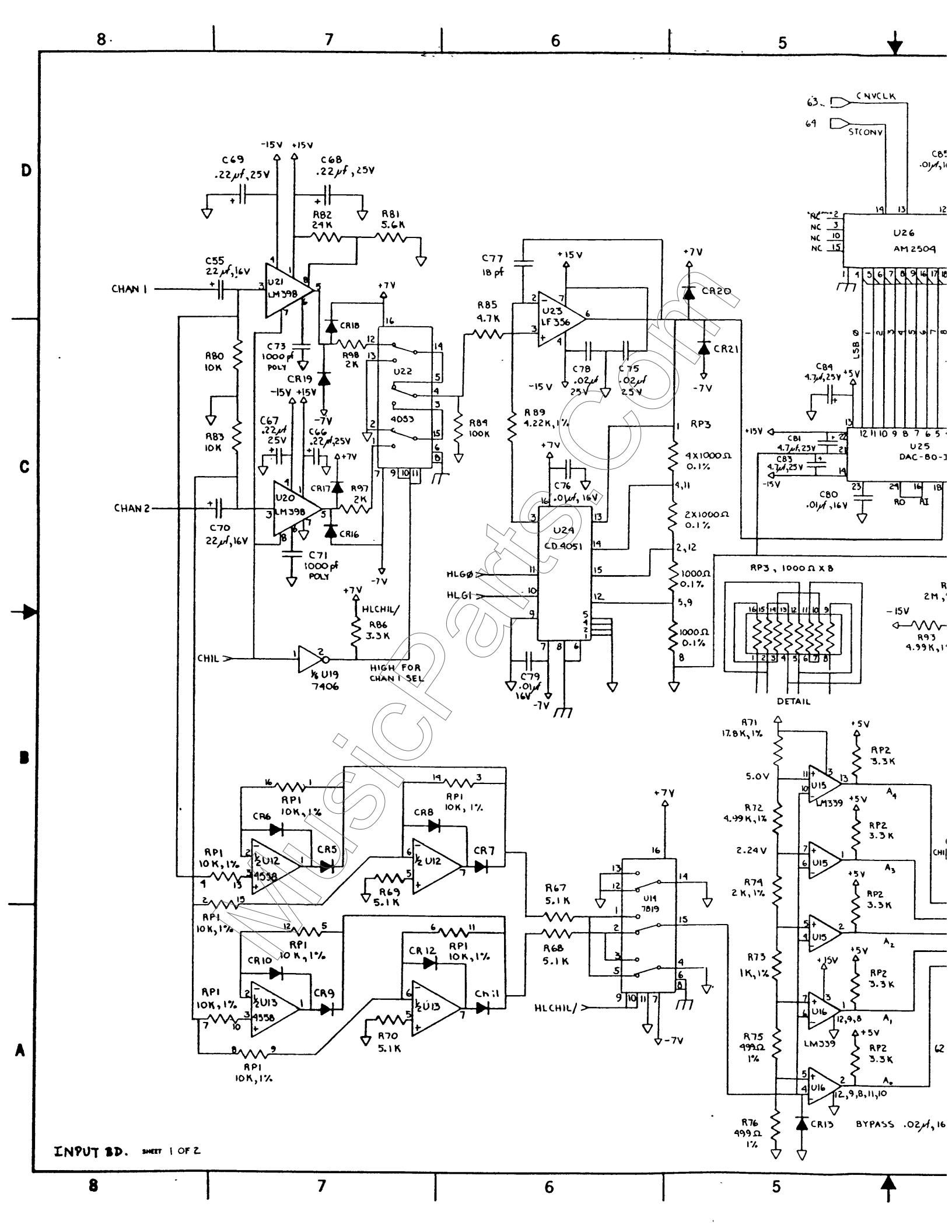
DATA MEMORY AND I/O - MODEL 224

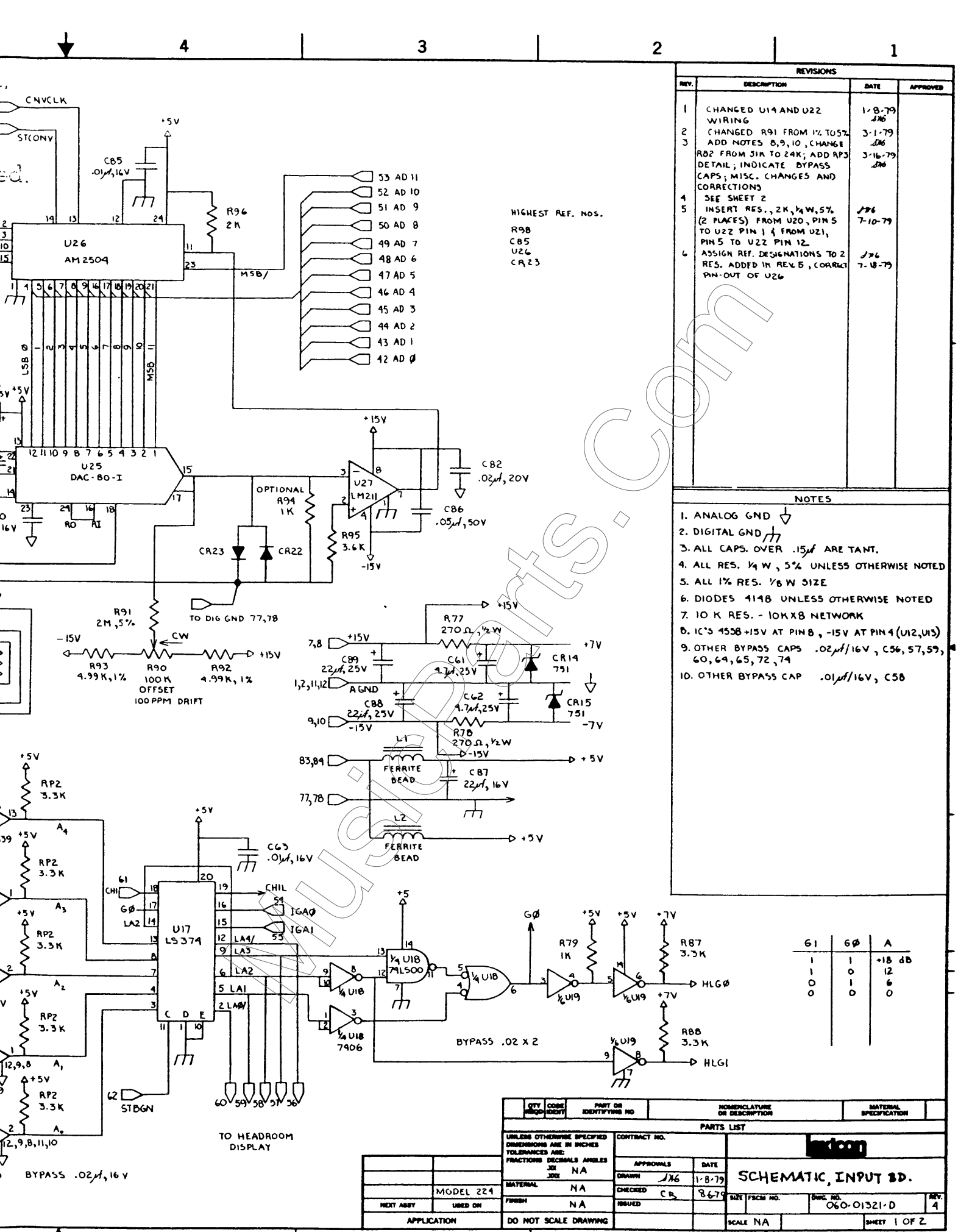
SHEET 2 OF 2

DRAWING NUMBER 060-01319



POWER SUPPLY


CHAN 1
CHAN 2
C69 .22µf,25V
C68 .22µf,25V
R82 24K
R81 5.6K
C55 22µf,16V
U21 LM398
U20 LM398
C70 22µf,16V
C71 1000pf POLY
C73 1000pf POLY
C67 .22µf 25V
C66 .22µf,25V
R80 10K
R83 10K
CR18
CR19
CR17
CR16
R98 2K
R97 2K
U22 4053
R89 100K
C77 18pf
U23 LF356
R85 4.7K
C78 .02µf 25V
C75 .02µf 25V
CR20
CR21
R89 4.22K,1%
C76 .01µf,16V
U24 CD4051
HLGØ
HLG1
C79 .01µf 16V
RP3
4X1000Ω 0.1%
2X1000Ω 0.1%
1000Ω 0.1%
1000Ω 0.1%
RP3, 1000Ω X 8
DETAIL
R93 4.99K,1%
2M
CHIL
R86 3.3K
1/6 U19 7406
HIGH FOR CHAN 1 SEL
HLCHIL/
RP1 10K,1%
CR6
CR5
CR8
CR7
½ U12 4538
R69 5.1K
R70 5.1K
CR10
CR9
CR12
CR11
½ U13 4538
R67 5.1K
R68 5.1K
U14 7819
R71 17.8K,1%
R72 4.99K,1%
R74 2K,1%
R73 1K,1%
R75 499Ω 1%
R76 499Ω 1%
5.0V
2.24V
RP2 3.3K
U15 LM339
U16 LM339
A4
A3
A2
A1
A0
CR13
BYPASS .02µf,16
63 CNVCLK
69 ST(ONV)
U26 AM2509
LSB Ø
C84 4.7µf,25V
C81 4.7µf,25V
C83 4.7µf,25V
C80 .01µf,16V
U25 DAC-80-1
RO
AI
+15V
-15V
+7V
-7V
+5V
INPUT BD. SHEET 1 OF 2



REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1	CHANGED U19 AND U22 WIRING	1-8-79 JM6	
2	CHANGED R91 FROM 1% TO 5%	3-1-79	
3	ADD NOTES 8,9,10, CHANGE R82 FROM 31K TO 24K; ADD RP3 DETAIL; INDICATE BYPASS CAPS; MISC. CHANGES AND CORRECTIONS	3-16-79 JM6	
4	SEE SHEET 2		
5	INSERT RES., 2K, ¼W, 5% (2 PLACES) FROM U20, PIN 5 TO U22 PIN 1 & FROM U21, PIN 5 TO U22 PIN 12	JM6 7-10-79	
6	ASSIGN REF. DESIGNATIONS TO 2 RES. ADDED IN REV 5, CORRECT PIN-OUT OF U26	JM6 7-18-79	

NOTES

1. ANALOG GND
2. DIGITAL GND
3. ALL CAPS. OVER .15μf ARE TANT.
4. ALL RES. ¼ W, 5% UNLESS OTHERWISE NOTED
5. ALL 1% RES. ⅛ W SIZE
6. DIODES 4148 UNLESS OTHERWISE NOTED
7. 10 K RES. - 10KX8 NETWORK
8. IC'S 4558 +15V AT PIN 8, -15V AT PIN 4 (U12, U13)
9. OTHER BYPASS CAPS .02μf/16V, C56, 57, 59, 60, 64, 65, 72, 74
10. OTHER BYPASS CAP .01μf/16V, C58

G1	GØ	A
1	1	+18 dB
1	0	12
0	1	6
0	0	0

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX NA .XXX

MATERIAL NA

FINISH NA

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN JM6	1-8-79
CHECKED CB	8-6-79
ISSUED	

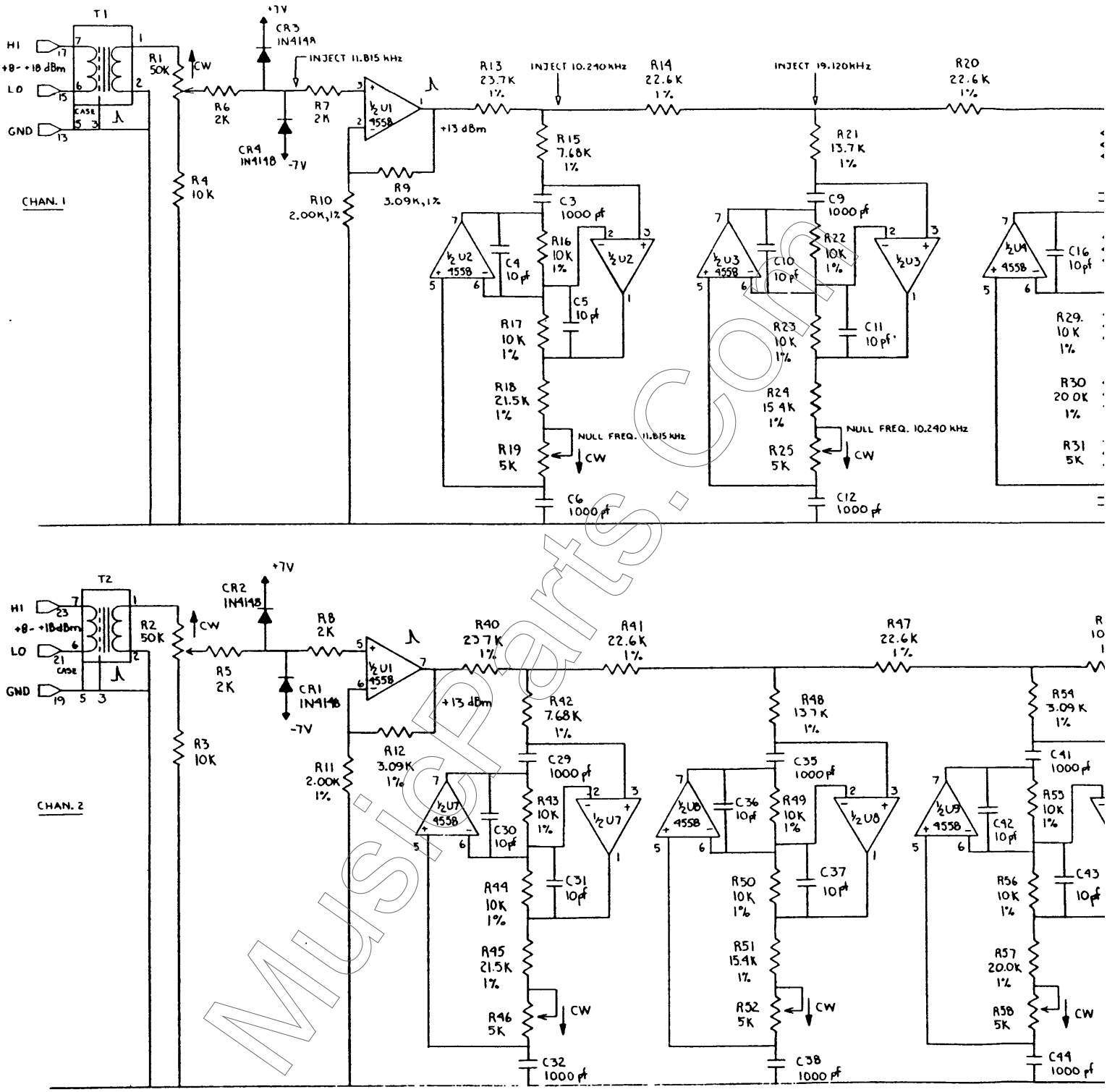
Intecom

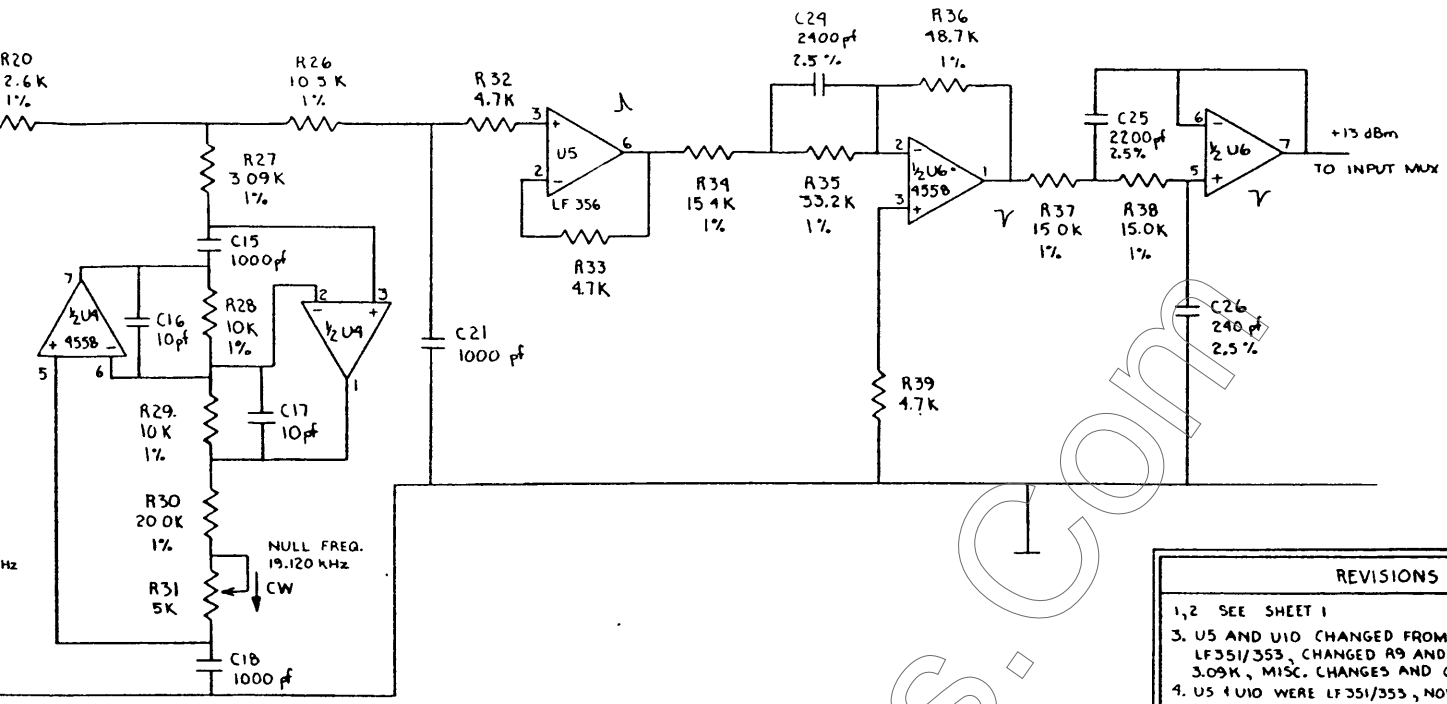
SCHEMATIC, INPUT BD.

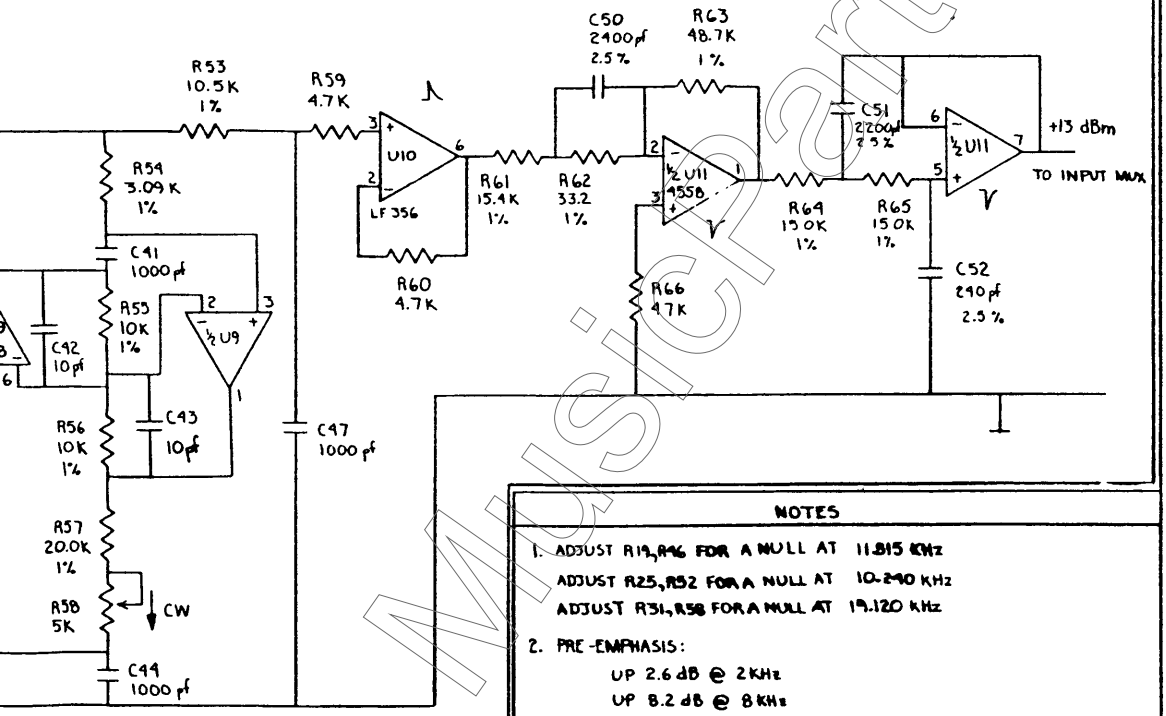
SIZE | FSCM NO. | DWG. NO. 060-01321-D | REV. 4

SCALE NA | SHEET 1 OF 2

MODEL 224	
NEXT ASSY	USED ON
APPLICATION	







REVISIONS

1,2 SEE SHEET 1

3. U5 AND U10 CHANGED FROM LM741 TO LF351/353, CHANGED R9 AND R12 FROM 2 3.09K, MISC. CHANGES AND CORRECTIONS

4. U5 & U10 WERE LF351/353, NOW LF356

5. SEE SHEET 1

NOTES

1. ADJUST R19,R46 FOR A NULL AT 11.815 KHz
   ADJUST R25,R52 FOR A NULL AT 10.290 KHz
   ADJUST R31,R58 FOR A NULL AT 19.120 KHz

2. PRE-EMPHASIS:
   UP 2.6 dB @ 2KHz
   UP 8.2 dB @ 8KHz

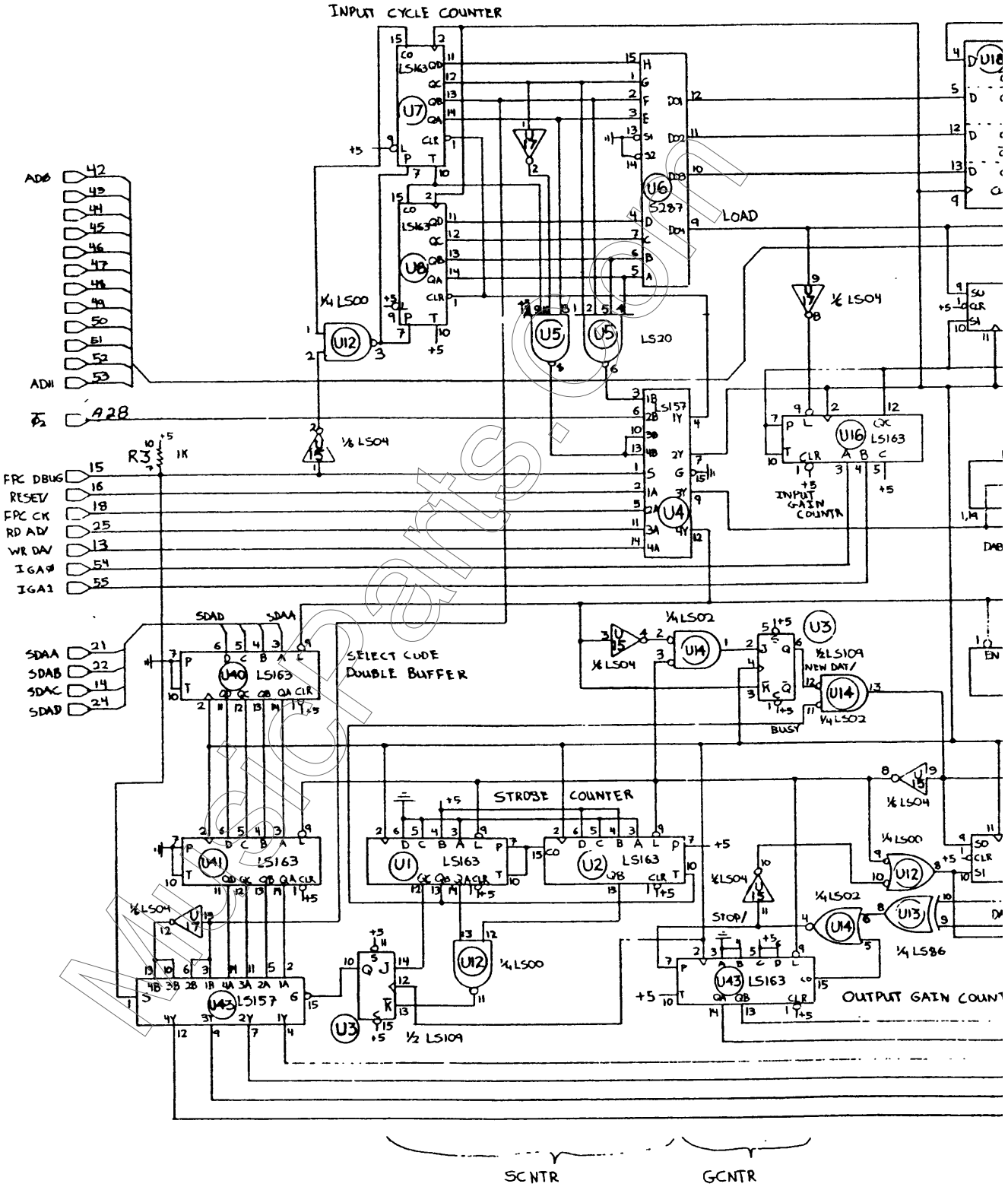
3. .02μf/16 BYPASS CAPS: C1,2,7,8,13,14,19,20,22,23,27,28,33,34, 39,40,45,46,48,49,53,54

LEXICON INC, WALTHAM MA

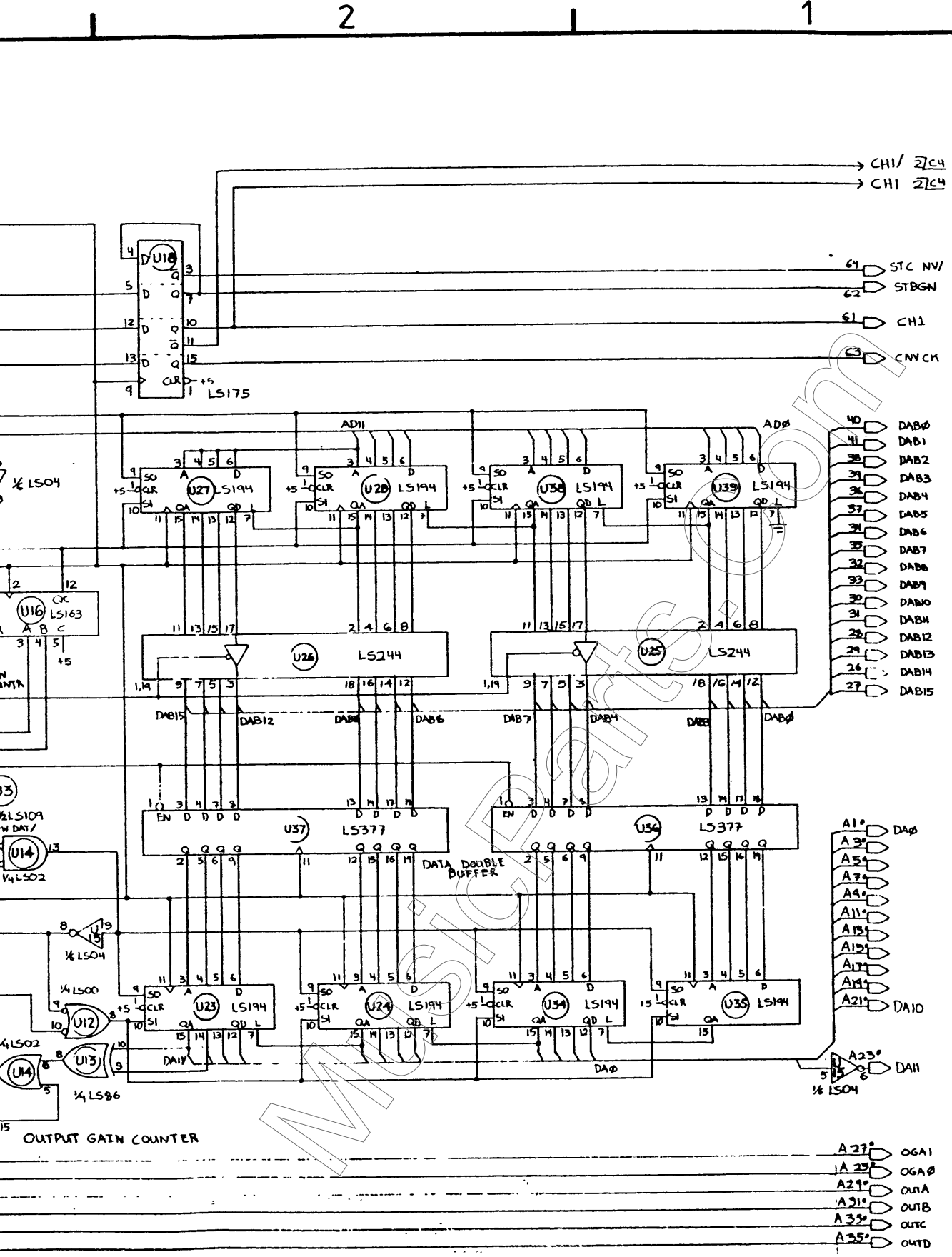
SCALE NA	APPROVED BY: CB 7-26-78	ASSEMBLY
DATE 12-28-78		REVISION

SCHEMATIC, INPUT BD., 224

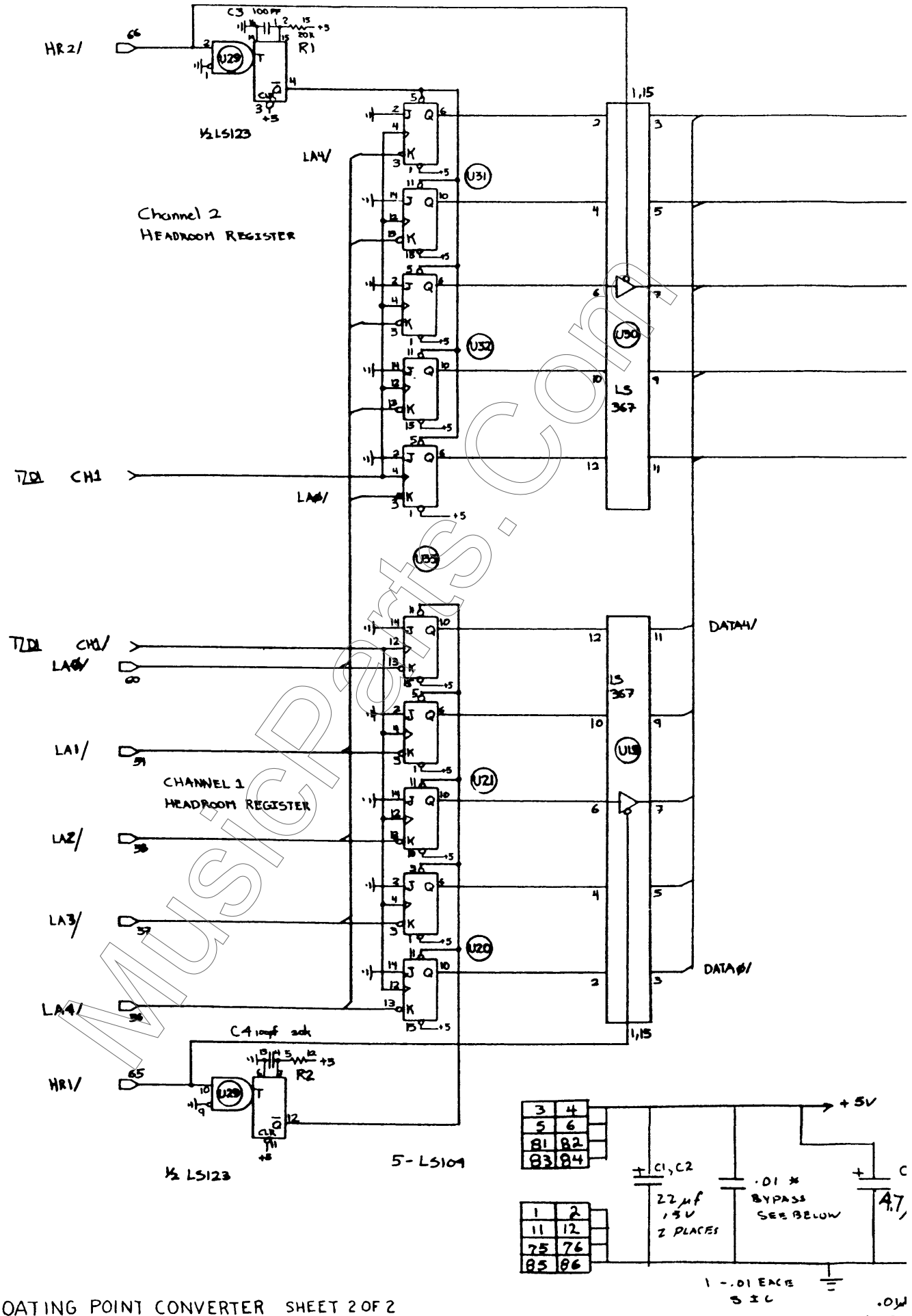
SHEET 2 OF 2 | DRAWING 060-



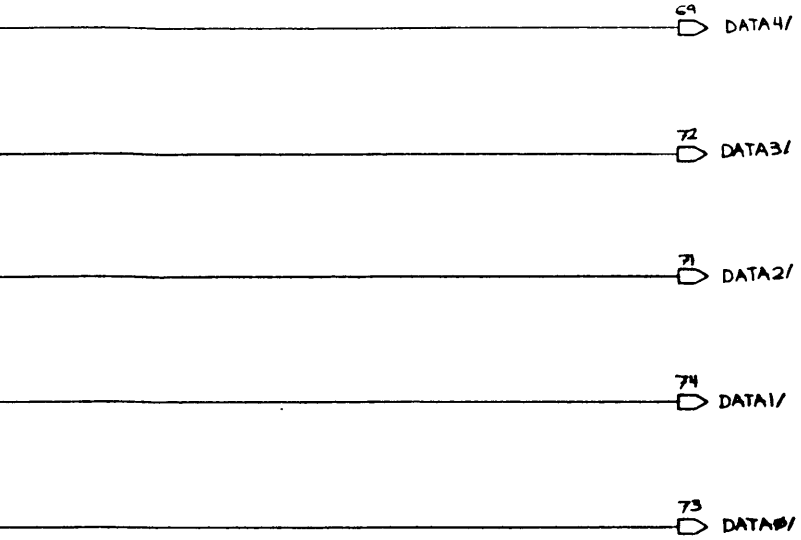
FLOATING POINT CONVERTER SHEET 1 OF 2



LEXICON INC, WALTHAM MA 02154		
SCALE: NA	APPROVED BY: CB.	DRAWN BY: R. KAO
DATE: 7-31-78		REVISED: 2/8-19-79
FLOATING POINT CONVERTER-MODEL 224		
SHEET 1 OF 2		DRAWING NO. 060-01320



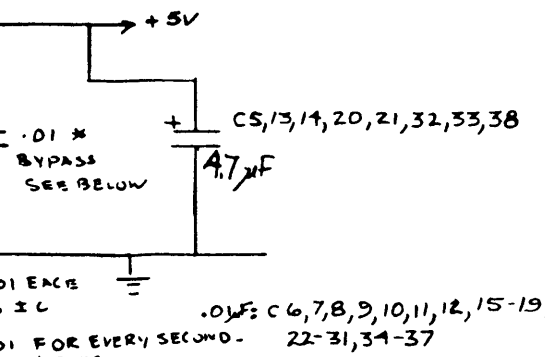
FLOATING POINT CONVERTER SHEET 2 OF 2



H/

6/

SPARE IC LOCATIONS:
U9,10,11,22,44



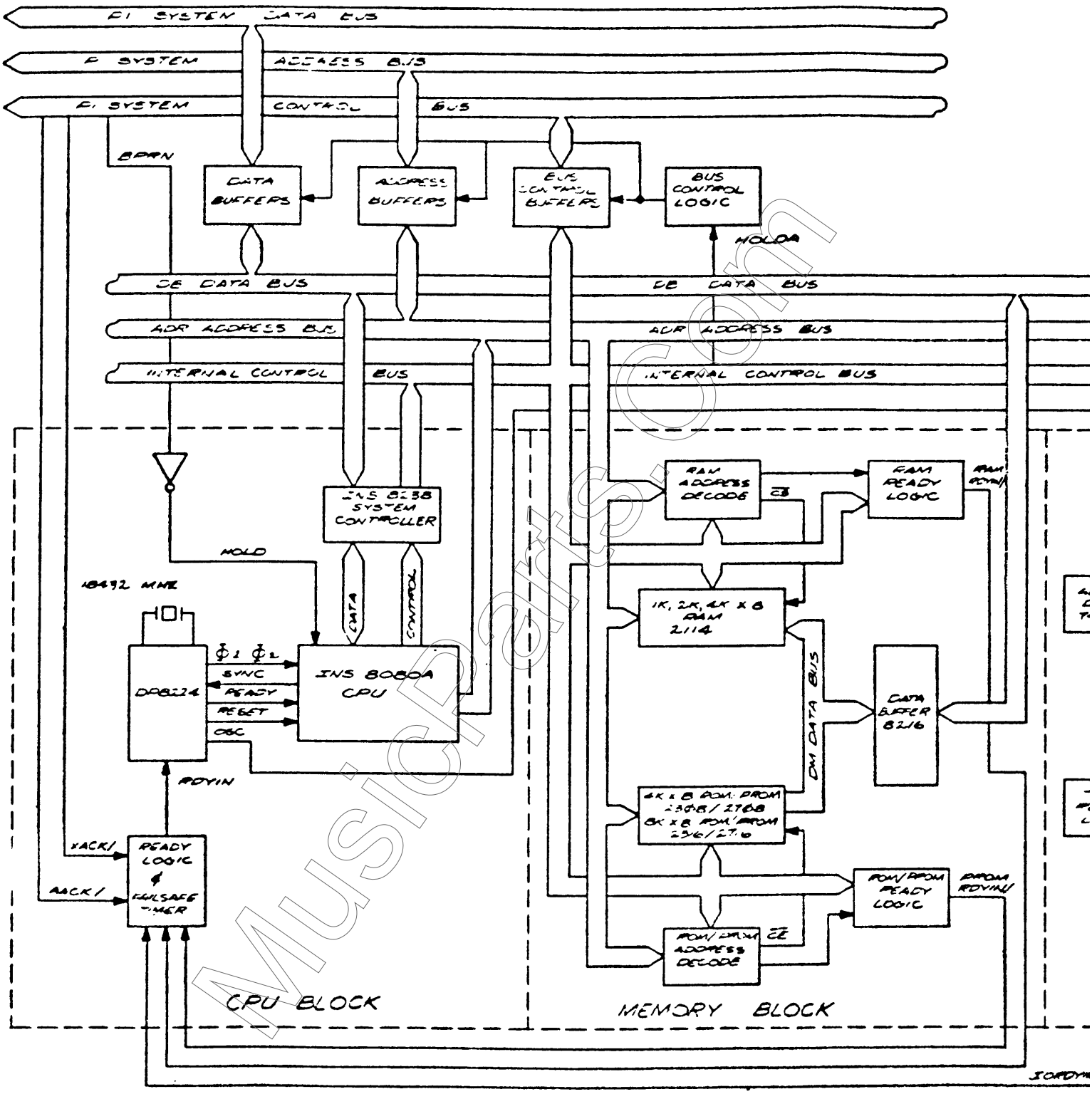
REV	DATE	DESCRIPTION	INIT.
2	8-14-79	LA4- LA6/ NOW LA6/ - LA4/	JTC

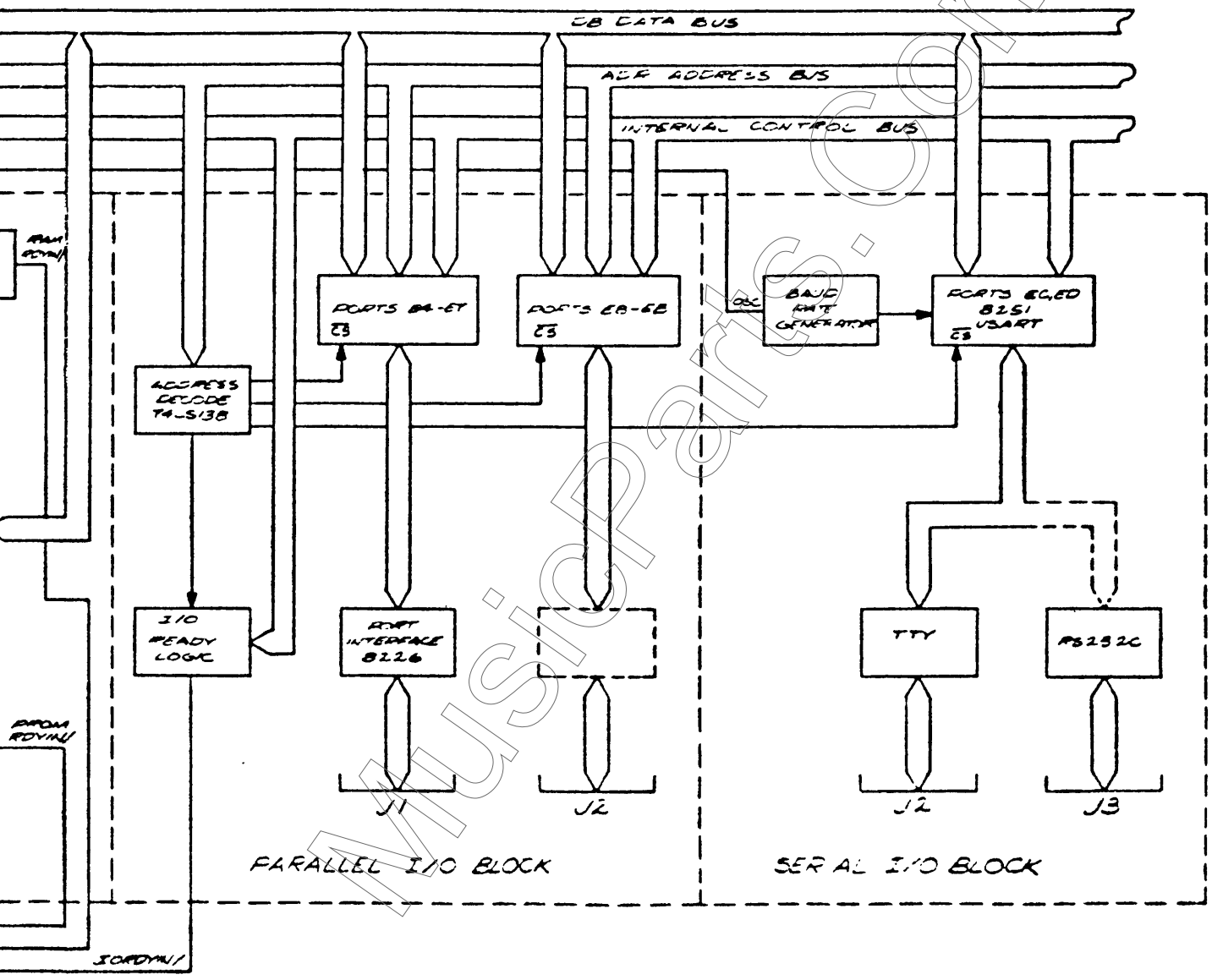
LEXICON INC, WALTHAM MA 02154

SCALE NA	APPROVED BY C.B.	DRAWN BY R. Kao
DATE 5/24/78		REVISED 8/ 8-14-79

FLOATING POINT CONVERTER- MODEL 224

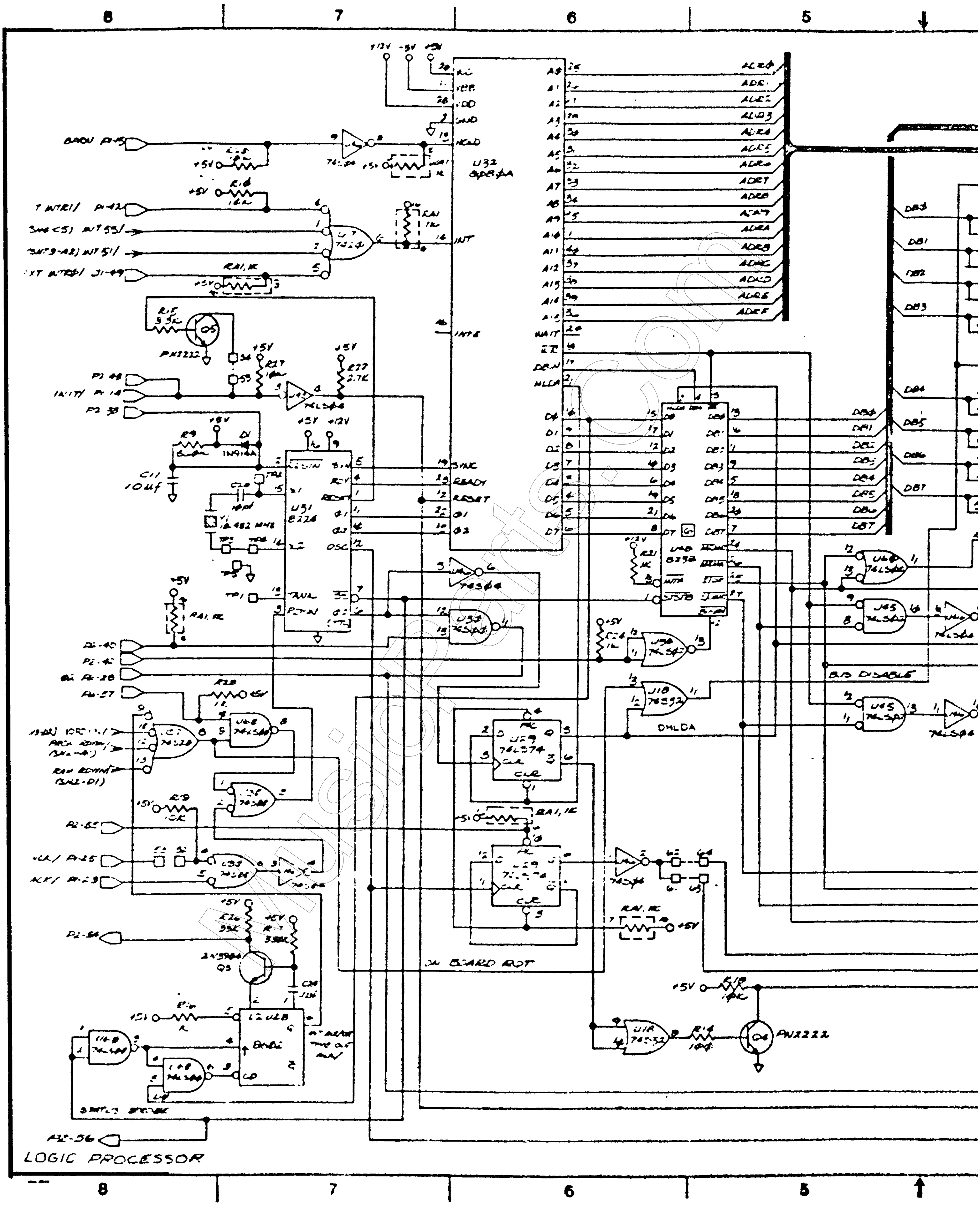
SHEET 2 OF 2 | DRAWING NUMBER 060-01320



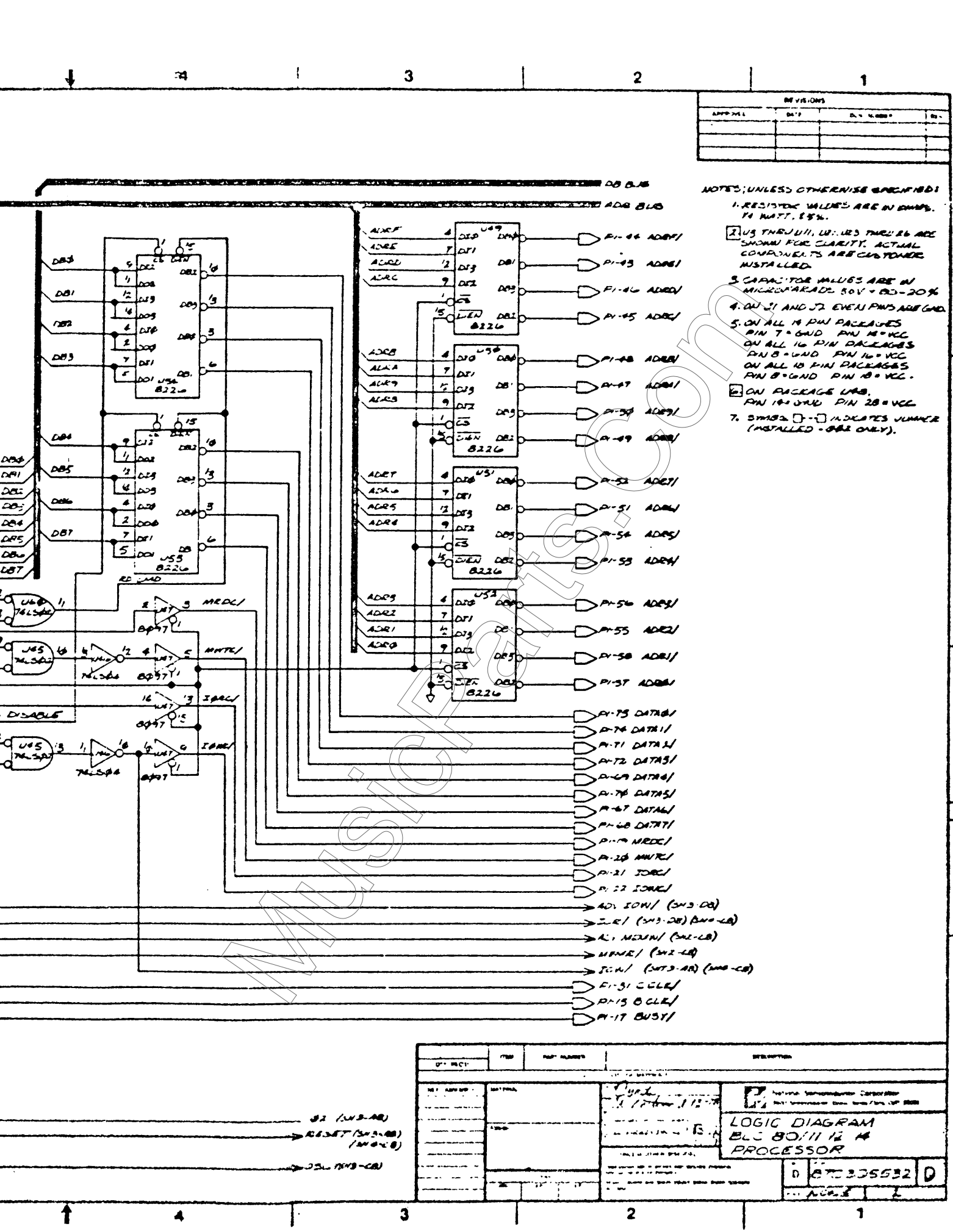


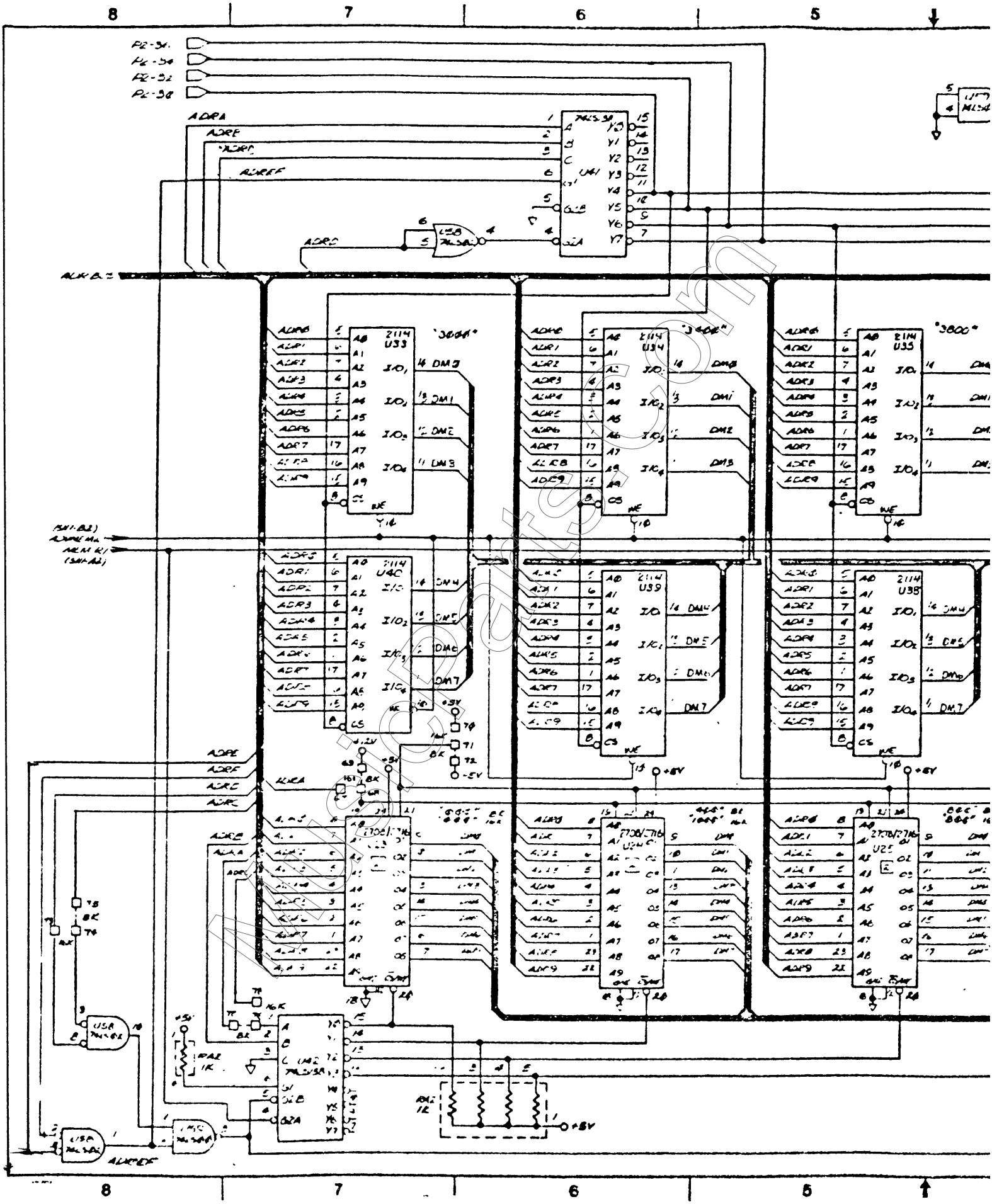
LOGIC DIAGRAM
ECB80 I/O, 2, MS
PROCESSOR

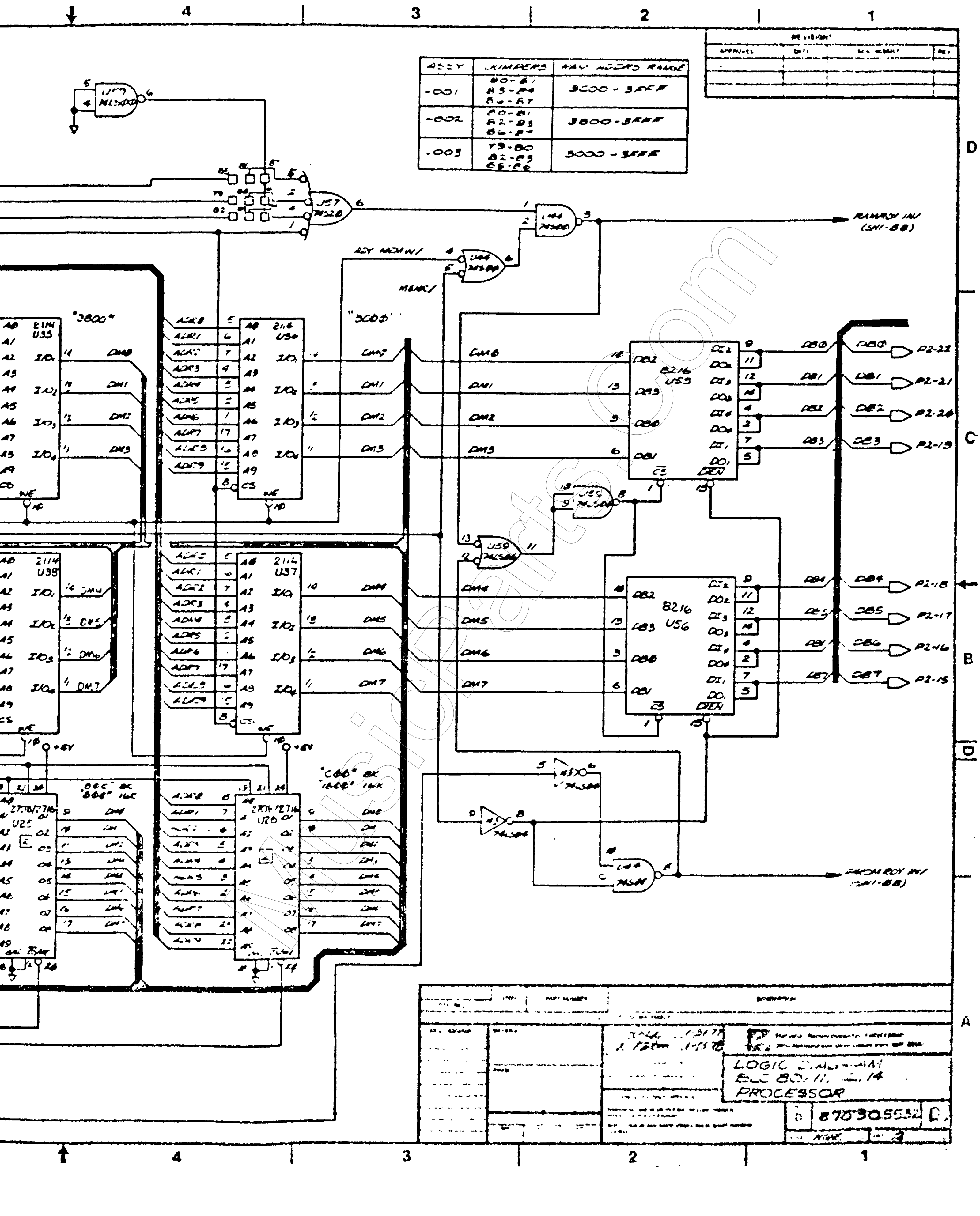
8700552



LOGIC PROCESSOR
U32
8080A
U31
8224
U28
8238
U29
74LS74
74LS04
74LS32
PN2222
IN914A
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
SYNC
READY
RESET
HOLD
INT
INTE
WAIT
HLDA
DBIN
BUS DISABLE
DHLDA
ON BOARD RQST
+5V
+12V
-5V


DB BUS
ADR BUS
NOTES; UNLESS OTHERWISE SPECIFIED:
1. RESISTOR VALUES ARE IN OHMS. 1/4 WATT, 5%.
2. U3 THRU U11, U8 - U13 THRU U16 ARE SHOWN FOR CLARITY. ACTUAL COMPONENTS ARE CUSTOMER INSTALLED.
3. CAPACITOR VALUES ARE IN MICROFARADS. 50V +80-20%
4. ON J1 AND J2 EVEN PINS ARE GND.
5. ON ALL 14 PIN PACKAGES PIN 7 = GND PIN 14 = VCC
ON ALL 16 PIN PACKAGES PIN 8 = GND PIN 16 = VCC
ON ALL 18 PIN PACKAGES PIN 9 = GND PIN 18 = VCC.
6. ON PACKAGE U8B, PIN 14 = GND PIN 28 = VCC
7. STRAP □-□ INDICATES JUMPER (INSTALLED - 8BE ONLY).
U55 8226
U56 8226
U57 8226
U58 8226
U59 8226
U60 8226
U61 8226
U62 8226
U63 8226
U64 74LS04
U65 74LS32
U66 74LS04
U67 8097
U68 74LS04
U65 74LS32
DISABLE
MRDC/
MWTC/
IORC/
IOWC/
AD1 IOW/ (SH3-DB)
INT/ (SH3-DB) (BUS-CB)
A1, MEMW/ (SH2-CB)
MEMR/ (SH2-CB)
IOR/ (SH3-AR) (BUS-CB)
P1-31 CCLK/
P1-13 BCLK/
P1-17 BUSY/
A1 (SH3-AR)
RESET (SH3-BB) (SH4-B)
DAL (SH3-CB)
LOGIC DIAGRAM
BLC 80/11 1/2 A
PROCESSOR
D
8TC335532
D

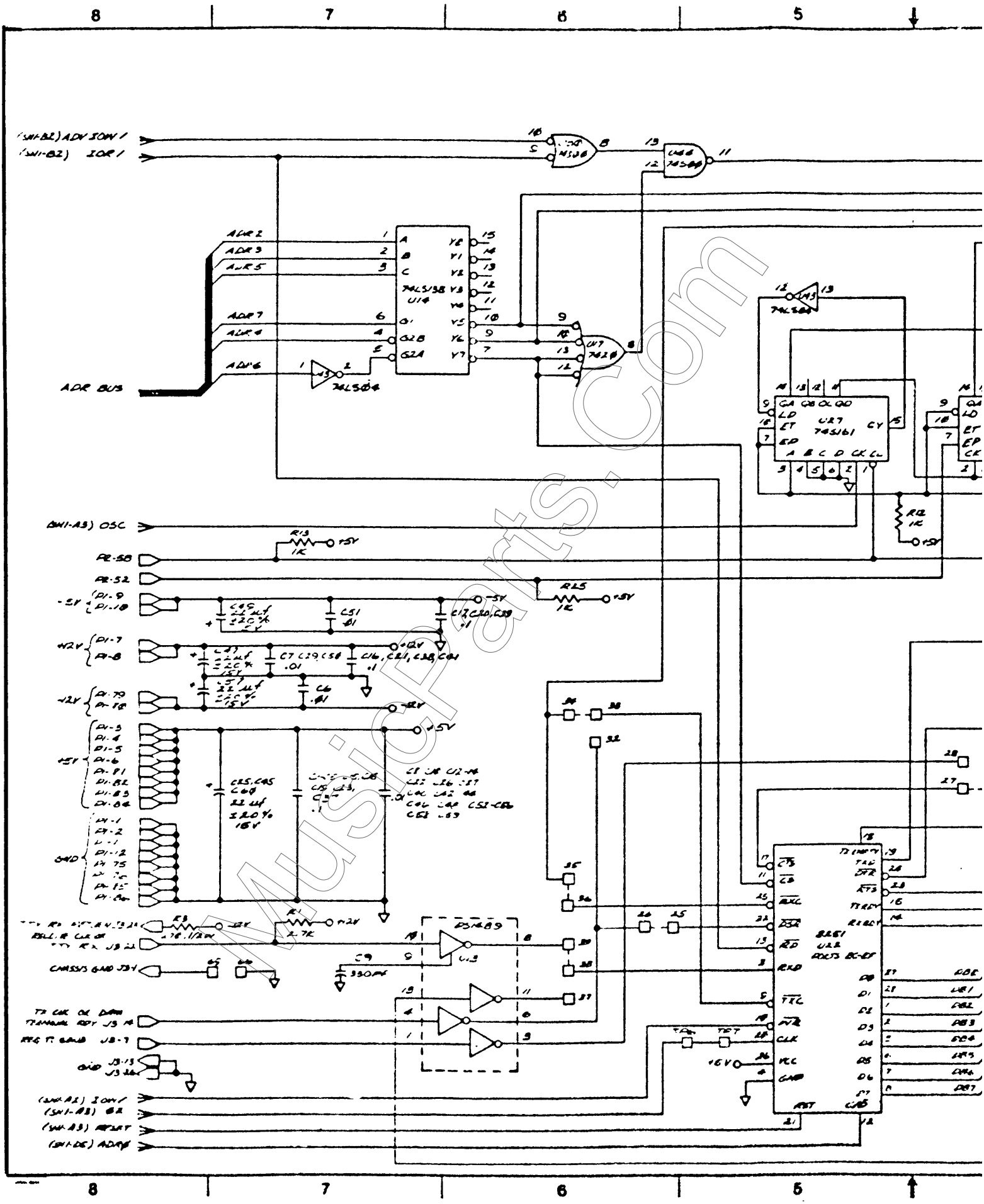

8
7
6
5
ADRA
ADRB
ADRC
ADREF
U41
74LS138
U33
U34
U35
U36
U37
U38
U39
U40
2114
"3000"
"3400"
"3800"
"3C00"
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
+5V
LOGIC PROCESSOR

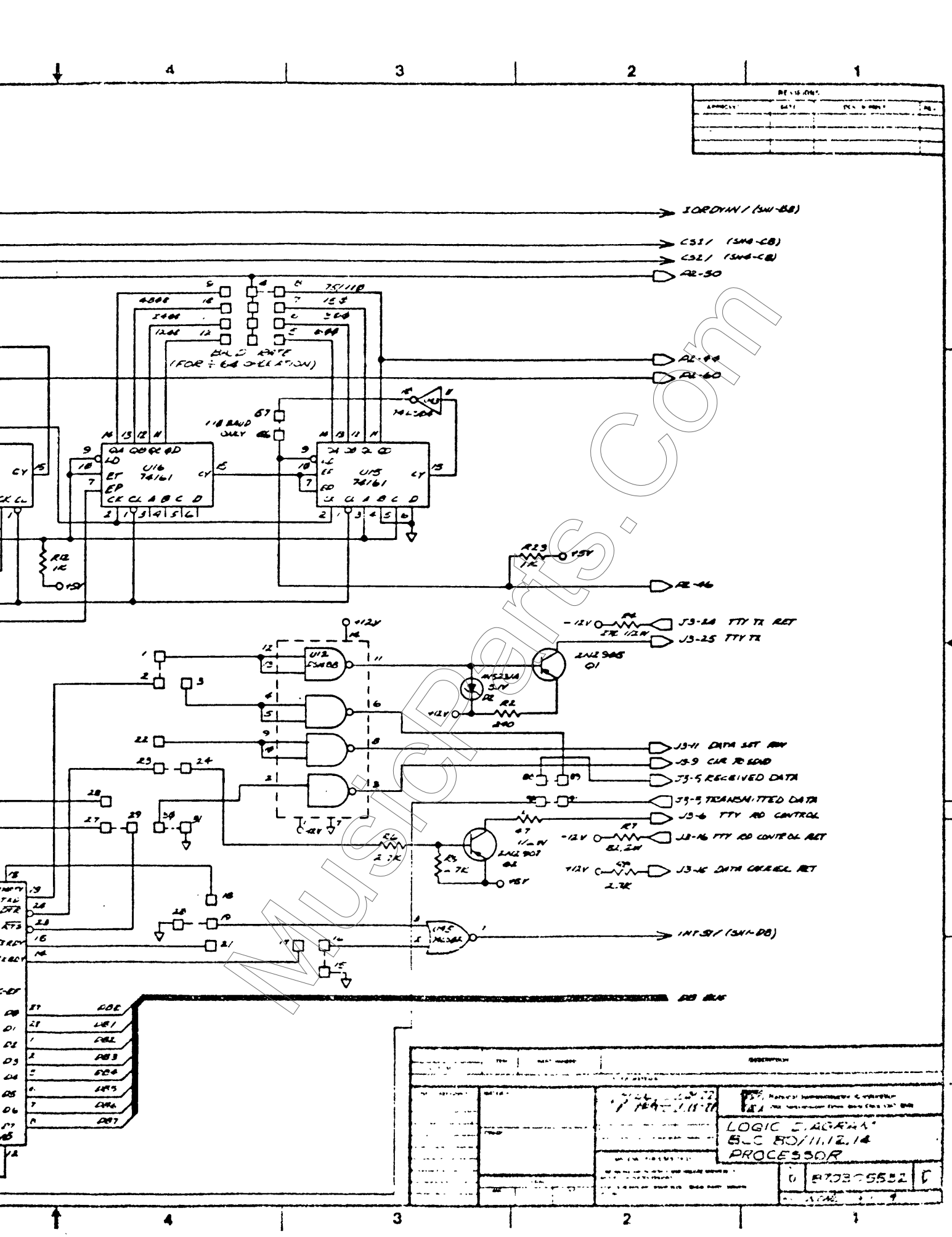


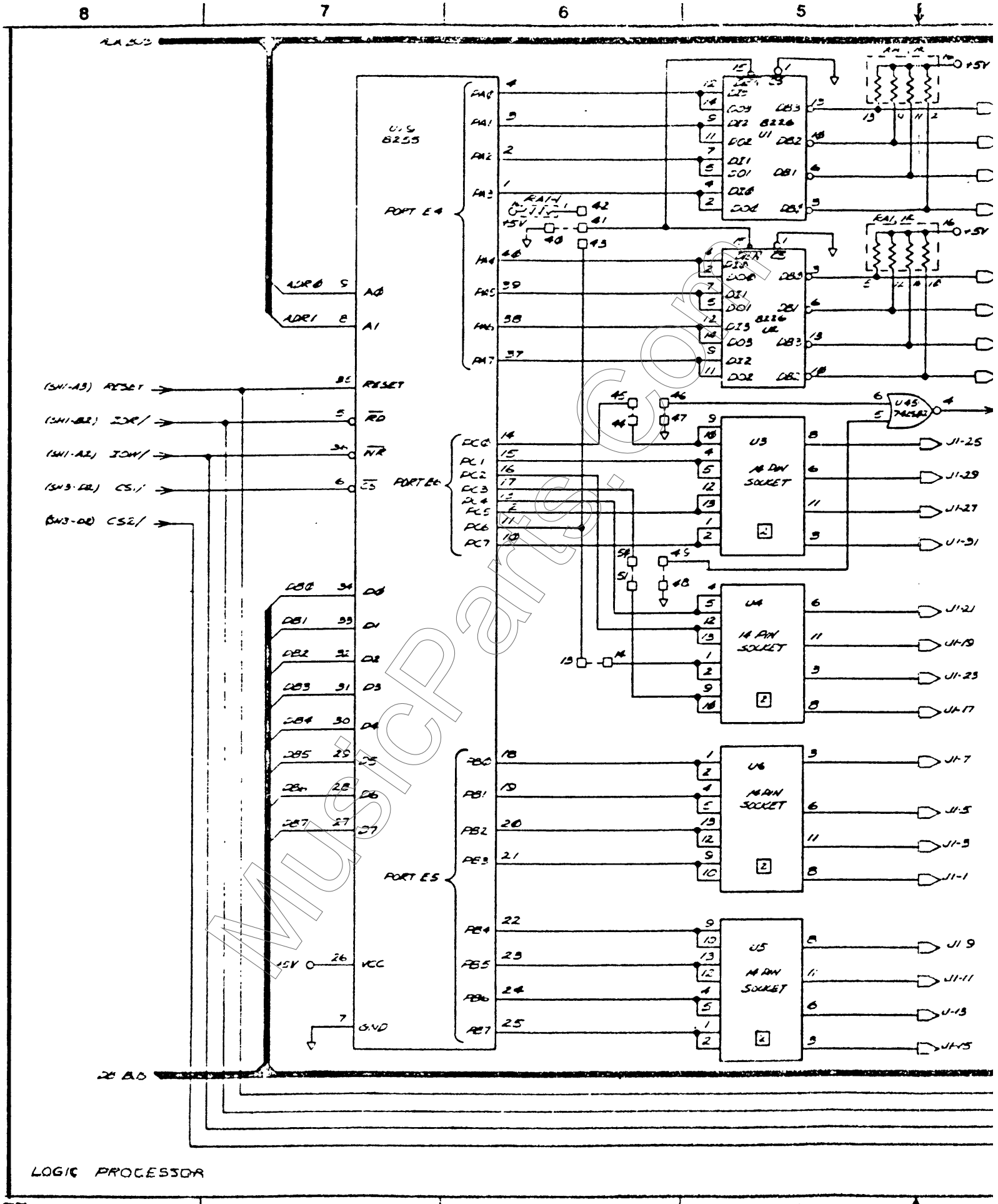
ASSY	JUMPERS	MAX ADDRS RANGE
-001	80-81, 83-84, 86-87	3C00 - 3FFF
-002	80-81, 82-83, 86-87	3800 - 3FFF
-003	79-80, 82-83, 85-86	3000 - 3FFF

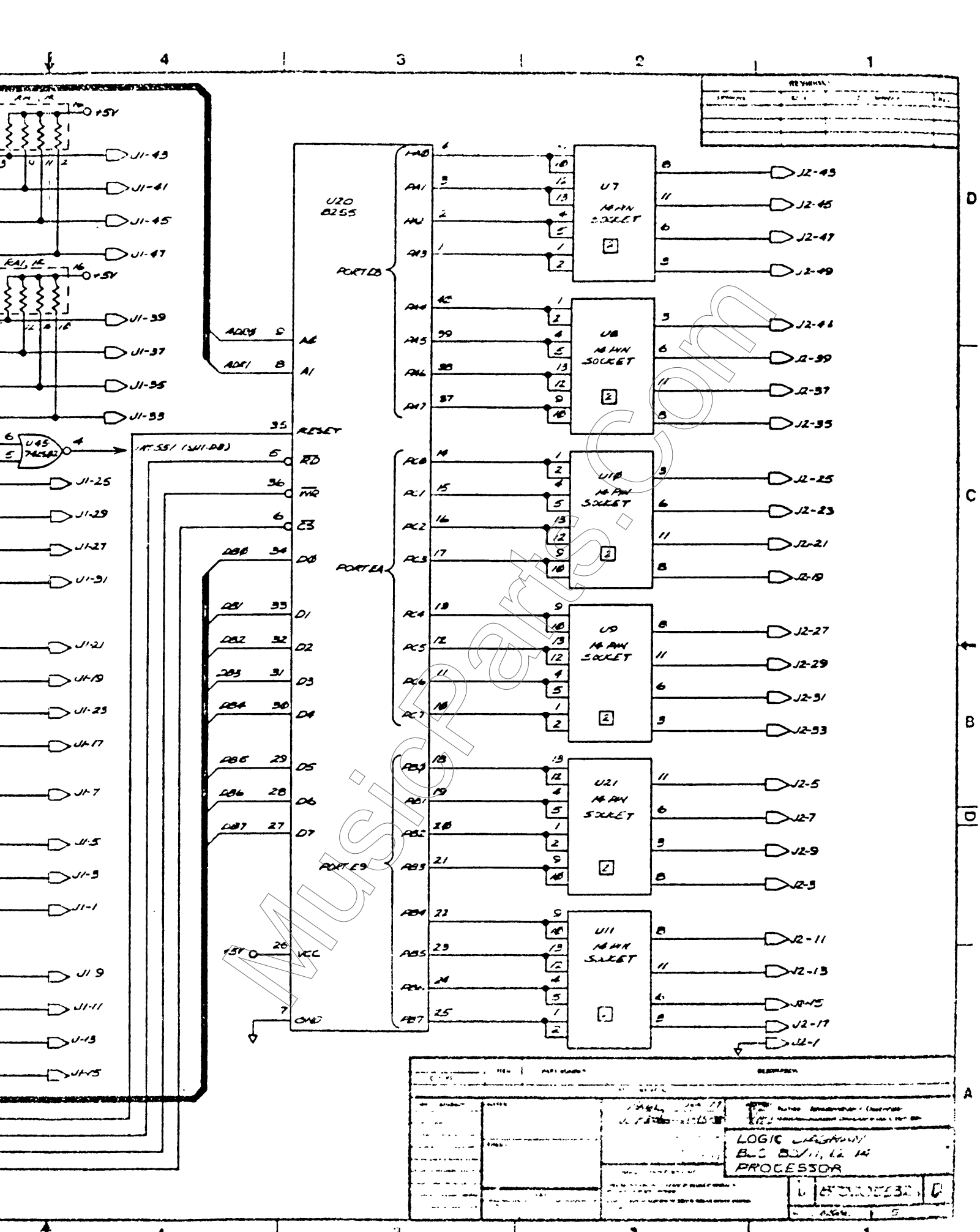
LOGIC DIAGRAM
ELC 80/11, 12, 14
PROCESSOR

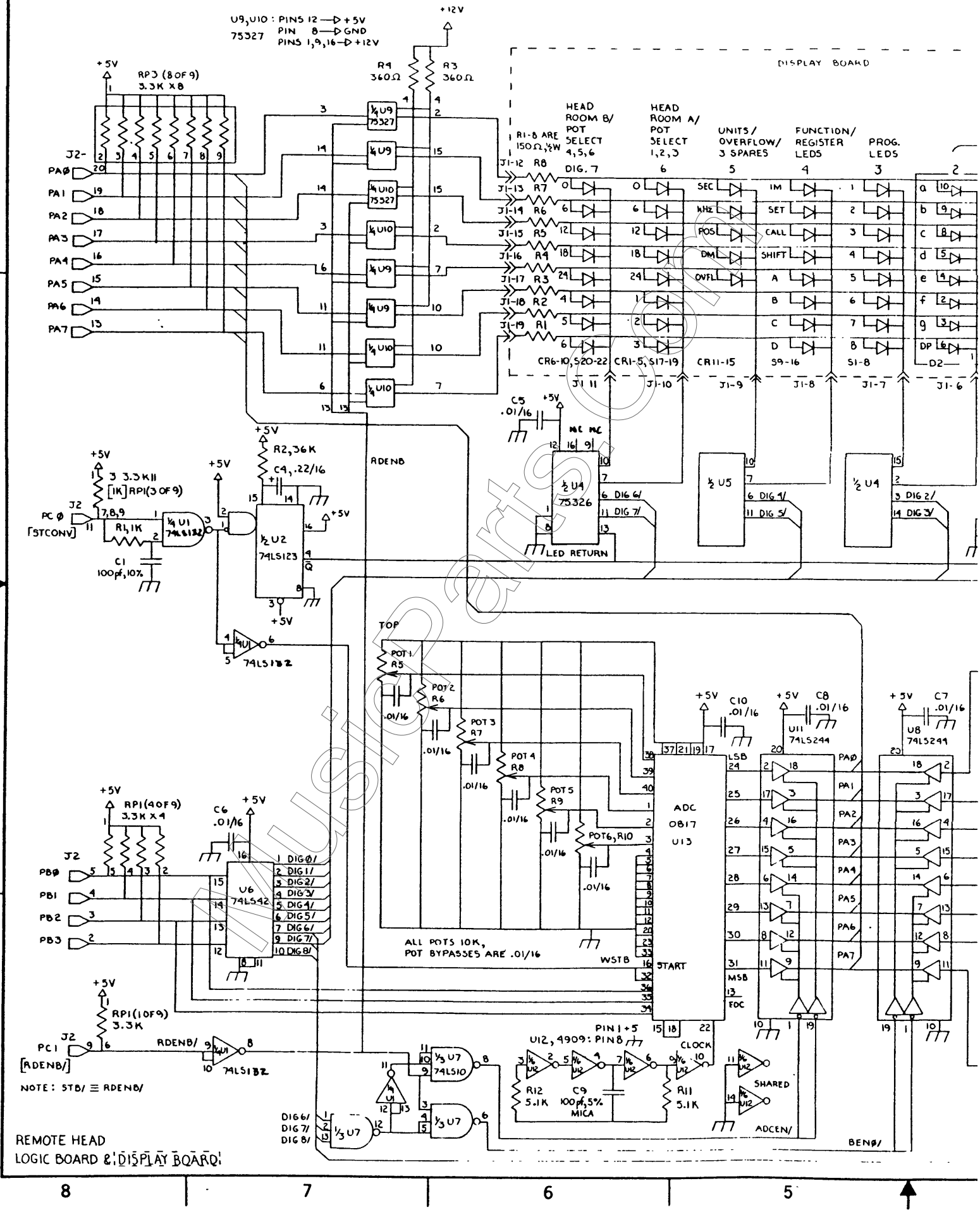
D 87030553 D

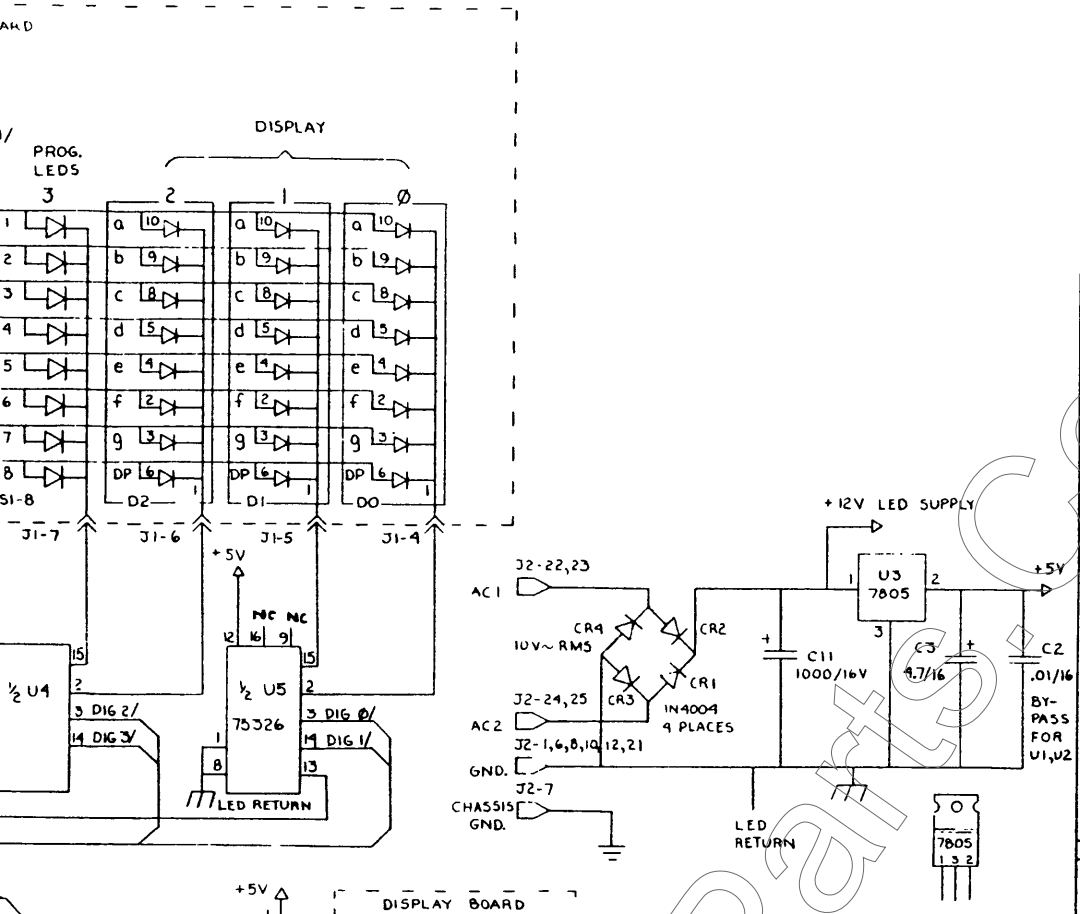


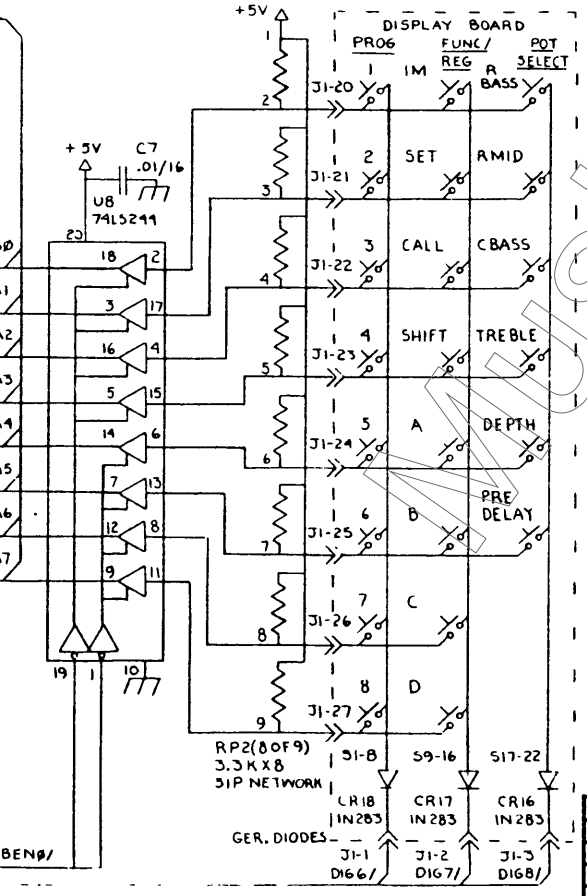







U9,U10 : PINS 12 → +5V
PIN 8 → GND
75327 PINS 1,9,16 → +12V
+12V
+5V
RP3 (8 OF 9)
3.3K X8
R4 360Ω
R3 360Ω
DISPLAY BOARD
HEAD ROOM B/ POT SELECT 4,5,6
HEAD ROOM A/ POT SELECT 1,2,3
UNITS/ OVERFLOW/ 3 SPARES
FUNCTION/ REGISTER LEDS
PROG. LEDS
R1-8 ARE 150Ω, ½W
DIG. 7
6
5
4
3
2
J2-
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
J1-12 R8
J1-13 R7
J1-14 R6
J1-15 R5
J1-16 R4
J1-17 R3
J1-18 R2
J1-19 R1
SEC
kHz
POS
DML
OVFL
IM
SET
CALL
SHIFT
A
B
C
D
a
b
c
d
e
f
g
DP
CR6-10, S20-22
CR1-5, S17-19
CR11-15
S9-16
S1-8
D2
J1 11
J1-10
J1-9
J1-8
J1-7
J1-6
C5 .01/16
NC NC
½ U4 75326
½ U5
½ U4
6 DIG 6/
11 DIG 7/
6 DIG 4/
11 DIG 5/
3 DIG 2/
14 DIG 3/
LED RETURN
3 3.3K Ω
[1K] RP1(3 OF 9)
PC0
[STCONV]
R1, 1K
C1 100pf, 10%
¼ U1 74LS132
½ U2 74LS123
R2, 36K
C4, .22/16
RDENB
+5V
TOP
POT 1 R5
POT 2 R6
POT 3 R7
POT 4 R8
POT 5 R9
POT6, R10
.01/16
ALL POTS 10K,
POT BYPASSES ARE .01/16
ADC 0817 U13
WSTB
START
MSB
EOC
LSB
C10 .01/16
C8 .01/16
C7 .01/16
U11 74LS244
U8 74LS244
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
RP1(4 OF 9)
3.3K X4
C6 .01/16
U6 74LS42
PB0
PB1
PB2
PB3
DIG 0/
DIG 1/
DIG 2/
DIG 3/
DIG 4/
DIG 5/
DIG 6/
DIG 7/
DIG 8/
RP1(1 OF 9)
3.3K
PC1
[RDENB/]
RDENB/
74LS132
NOTE: STB/ ≡ RDENB/
U12, 4909: PIN 8
PIN 1 + 5
CLOCK
R12 5.1K
C9 100pf, 5% MICA
R11 5.1K
SHARED
ADCEN/
BENB/
⅓ U7 74LS10
DIG6/
DIG7/
DIG8/
REMOTE HEAD
LOGIC BOARD & DISPLAY BOARD





MAX COMP #3
U13
R12
C11
CR18
RP3
J2
S22
D2

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1	REDRAWN JMG	3-14-79	
2	REDREW U4, U5 JMG	4-20-79	
3	ADD DIG GND & +5V TO U2 JMG CORRECT DWG. ERRORS ON S17-22 & DISPLAY DIG. Ø.	7-26-79	
4	FLOAT PINS 9 & 10 OF U4 & U5	10-8-79	
5	U1 WAS 74LS08, NOW 74LS132	10-16-79	

NOTES

1. CR1-15 ARE LED, LAMP, 5082-4980
2. S1-16 ARE SWITCH, LED, SCHADOW, DIGITAST, SRL, BLACK
3. S17-22 ARE SWITCH, LED, SCHADOW, DIGITAST, STL, BLACK
4. DØ-D2 ARE LED, DISPLAY, 5082-7613
5. ALL CAPS. IN μf UNLESS OTHERWISE NOTED
6. ALL RES. ¼W, 5% UNLESS OTHERWISE NOTED
7. BUS NOTES:

DENOTES BUS CONSISTING OF MULTIPLE AND SEPARATE LINES

2-45° BENDS INDICATES BUS CHANGE OF DIRECTION

CONNECTION

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX

CONTRACT NO.

	APPROVALS	DATE
DRAWN	JMG	3-14-79
CHECKED	CB	7-26-79
ISSUED		

MATERIAL
FINISH
NEXT ASSY
USED ON
MODEL 224
APPLICATION
DO NOT SCALE DRAWING

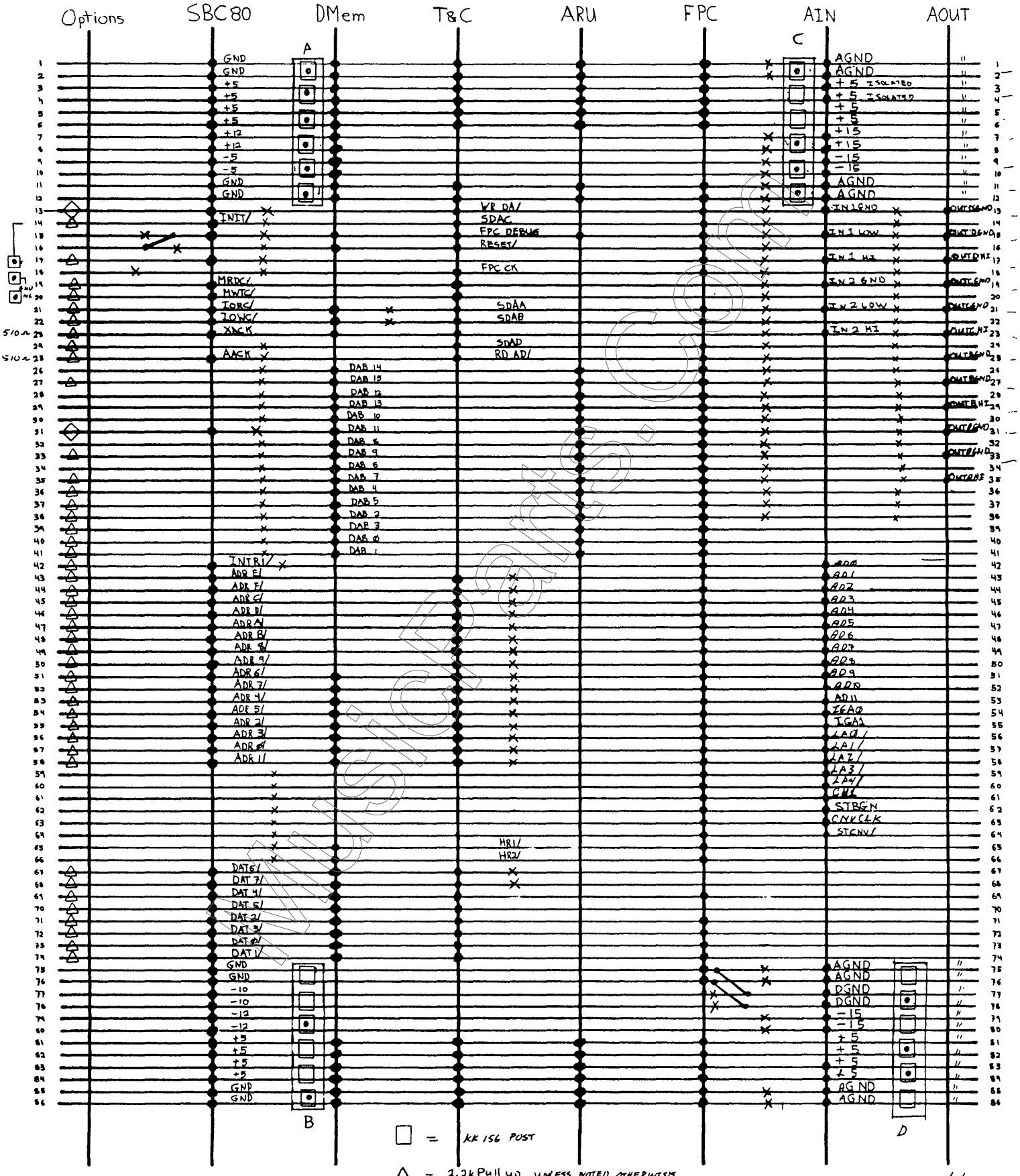
Ardcon

REMOTE HEAD
LOGIC BOARD & DISPLAY BOARD

SIZE | FSCM NO. | DWG. NO. 060-01323-D | REV 5
SCALE NA | SHEET 1 OF 1

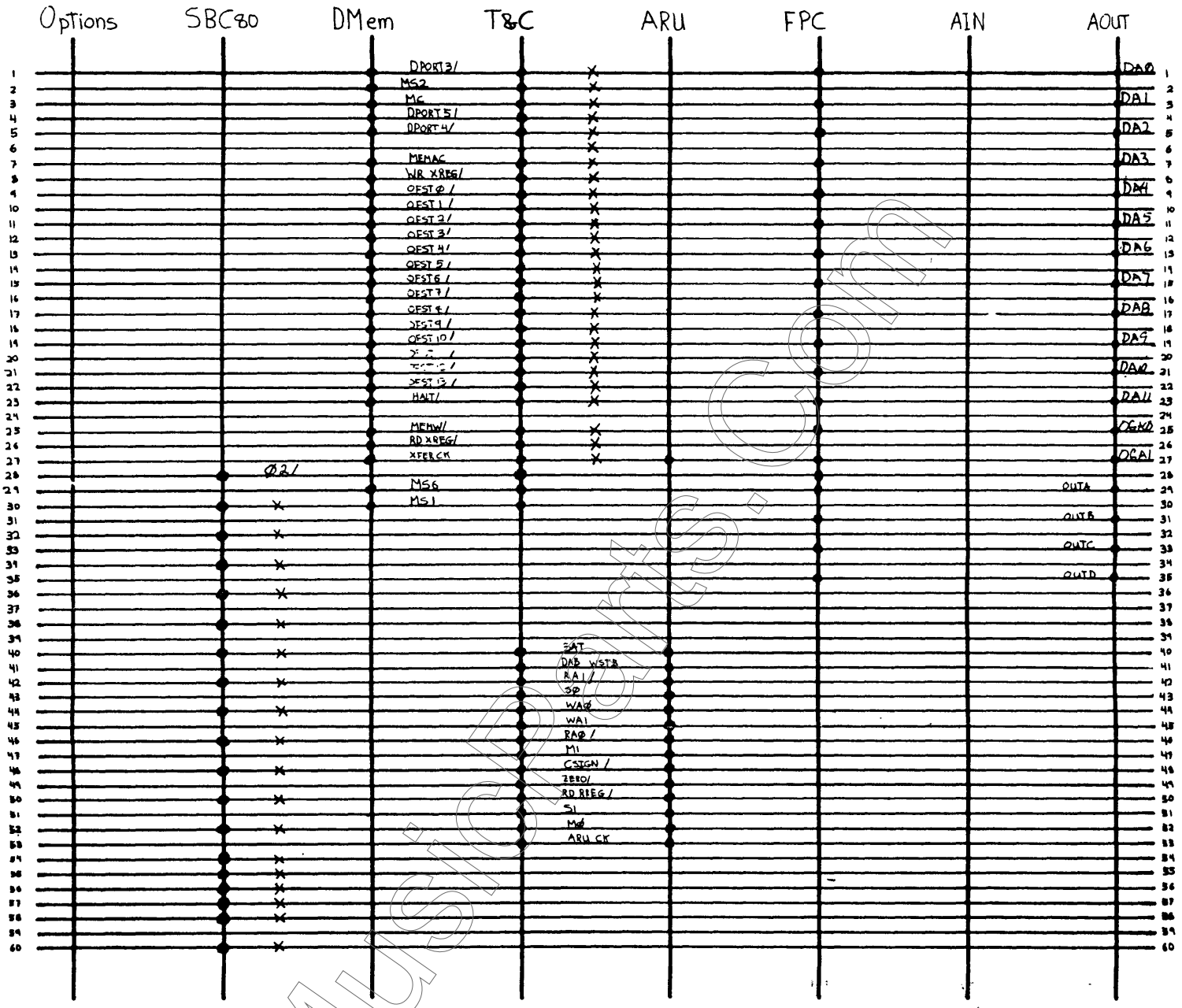
Model 224 Backplane Signals

Connector P1

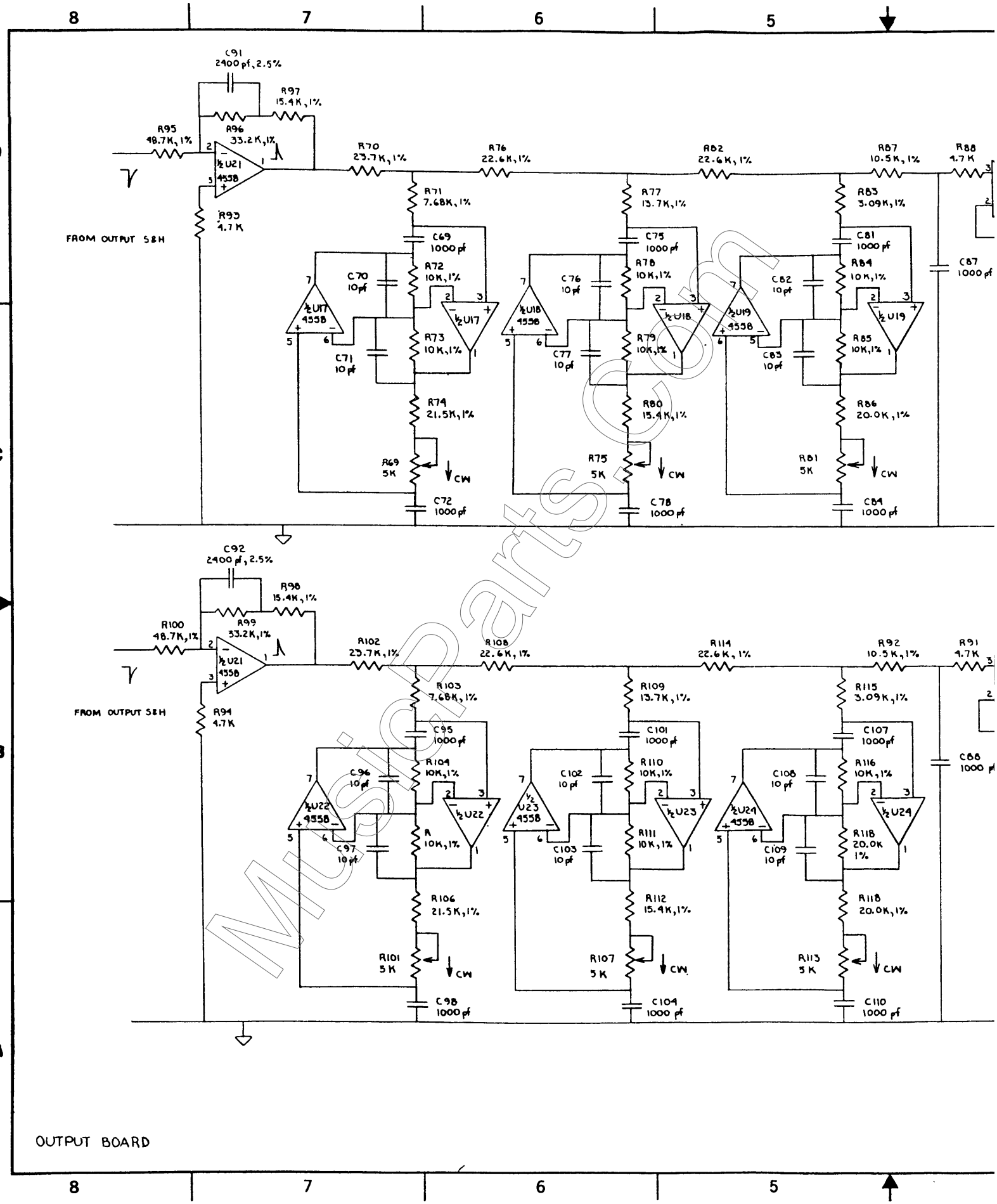


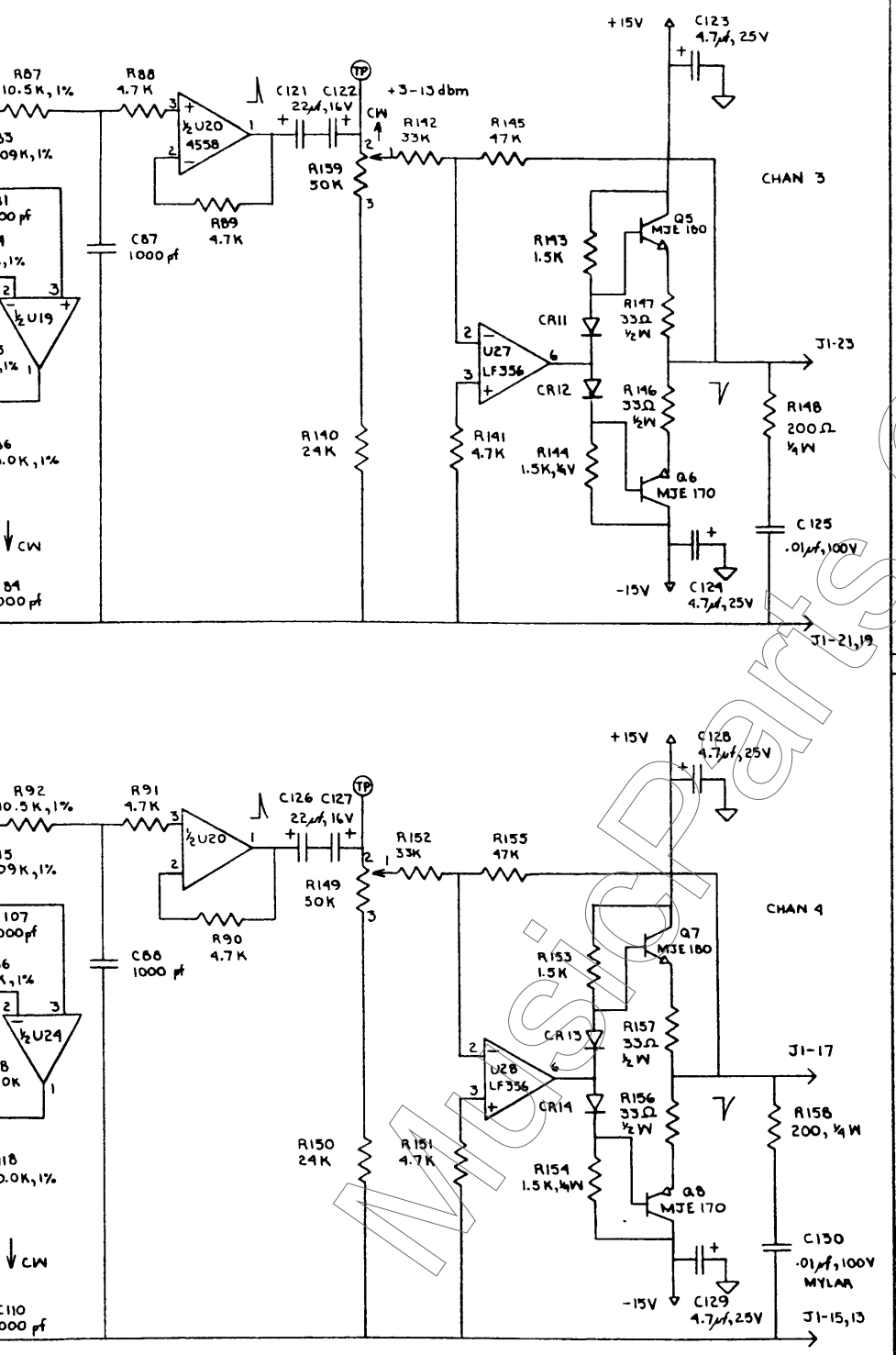
Model 224 Backplane Signals

Connector P2



REV - 10/11/78





REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1	CHANGE DWG. TITLE	8-31-79	

NOTES

1. ALL RESISTERS ARE 5%, ¼ W UNLESS OTHERWISE INDICATED.
2. ALL 1% RESISTERS ARE ⅛ W, METAL FILM
3. ALL 1000µf CAPACITORS ARE POLYPROPY
4. ALL DIODES ARE IN4148.
5. ADJUST R69, R101 FOR A NULL AT 11.815 kHz
   - - - R75, R107 - - - - 10.2398
   - - - R81, R113 - - - - 19.1204

QTY REQ	CODE IDENT NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

	224
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX NA
.XXX
MATERIAL NA
FINISH NA
DO NOT SCALE DRAWING

CONTRACT NO.

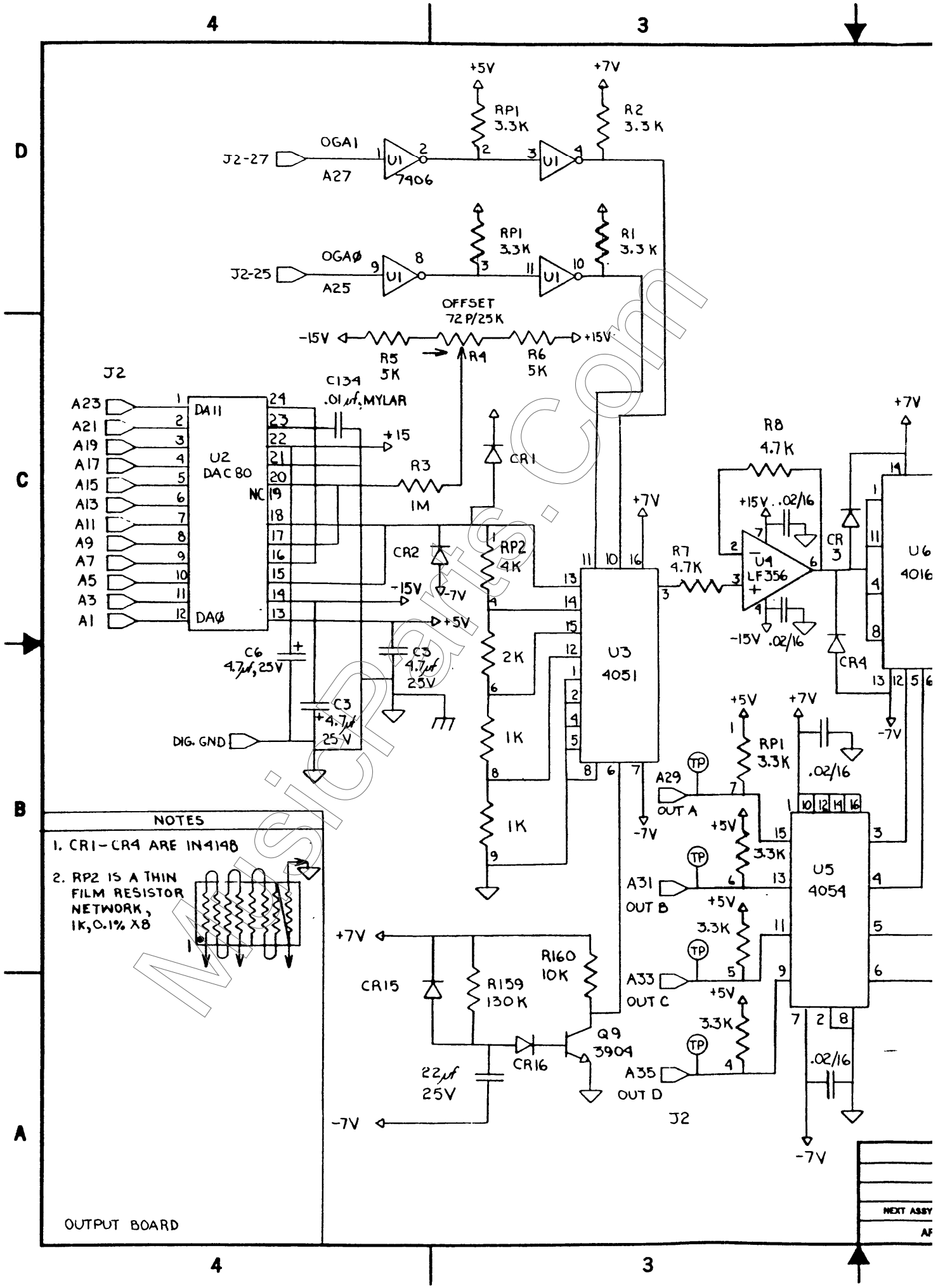
APPROVALS	DATE
DRAWN JAG	1-23-79
CHECKED CB	7-26-79
ISSUED	

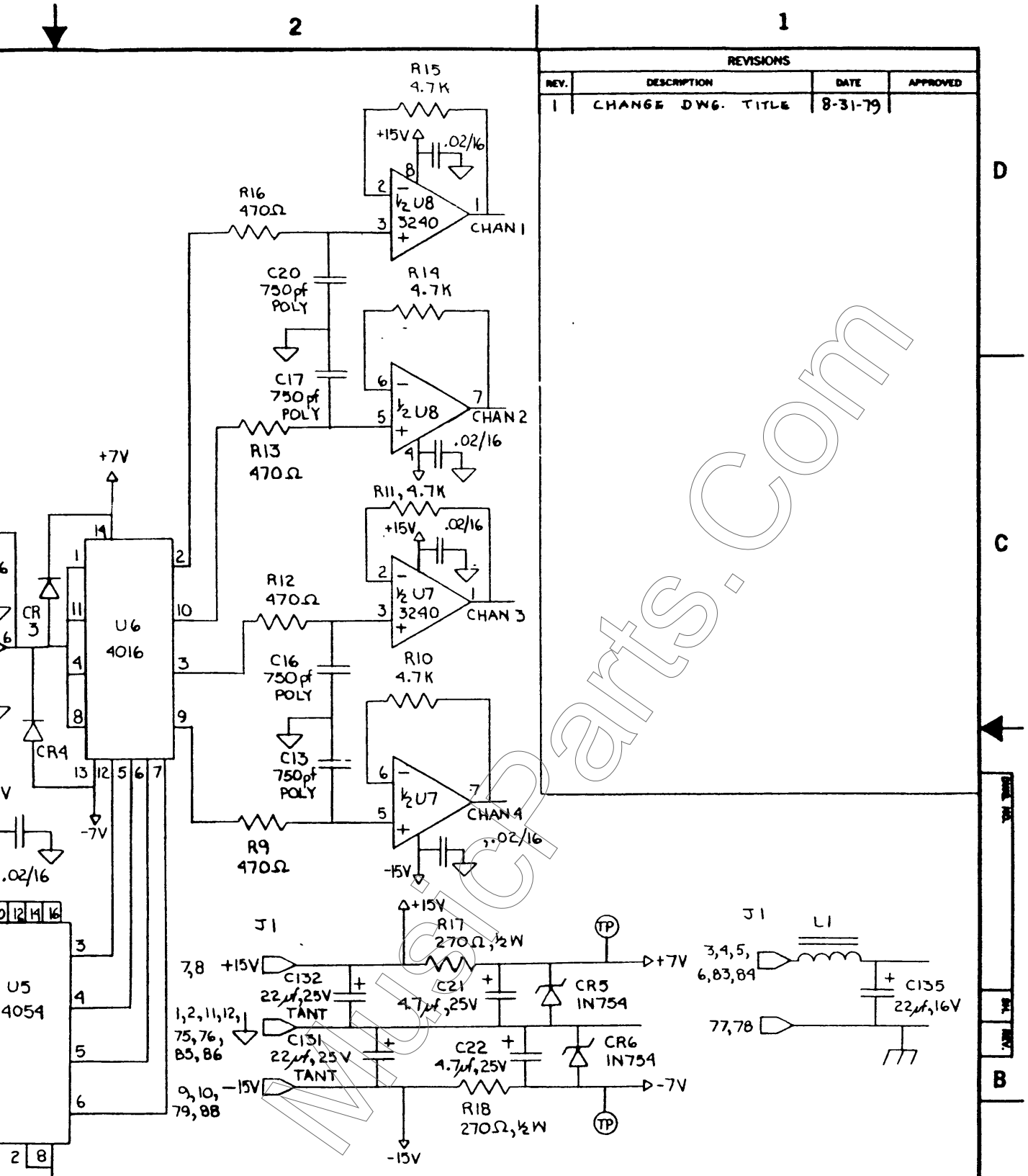
Tadiran

SCHEMATIC, OUTPUT BOARD, 224

SIZE D | FSCM NO. | DWG NO. 060-01322-D | REV. 1

SCALE NA | SHEET





QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

	224
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX NA
.XXX
MATERIAL NA
FINISH NA
DO NOT SCALE DRAWING

CONTRACT NO.

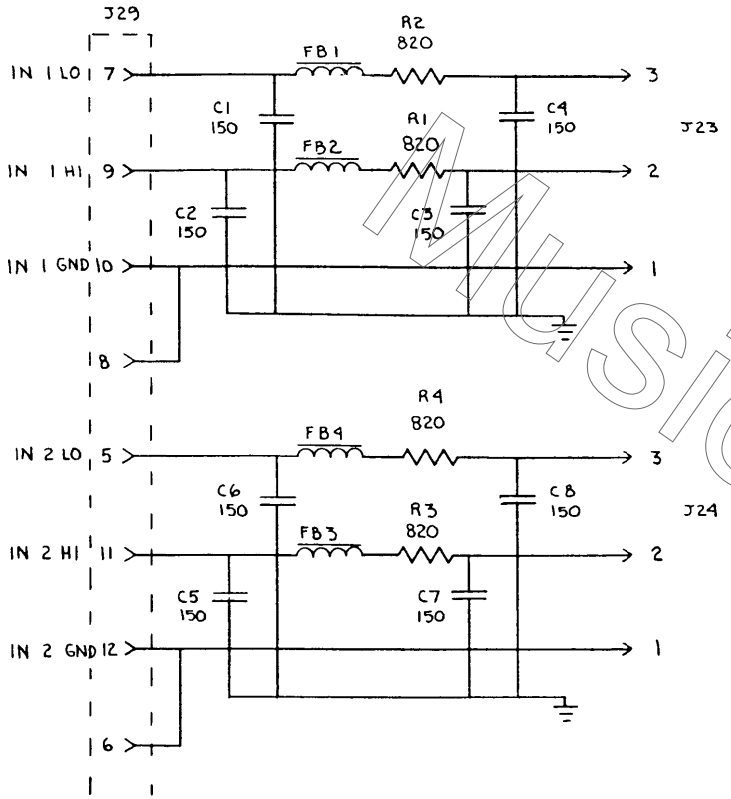
APPROVALS	DATE
DRAWN JAG	1-19-79
CHECKED RB	8-6-79
ISSUED	

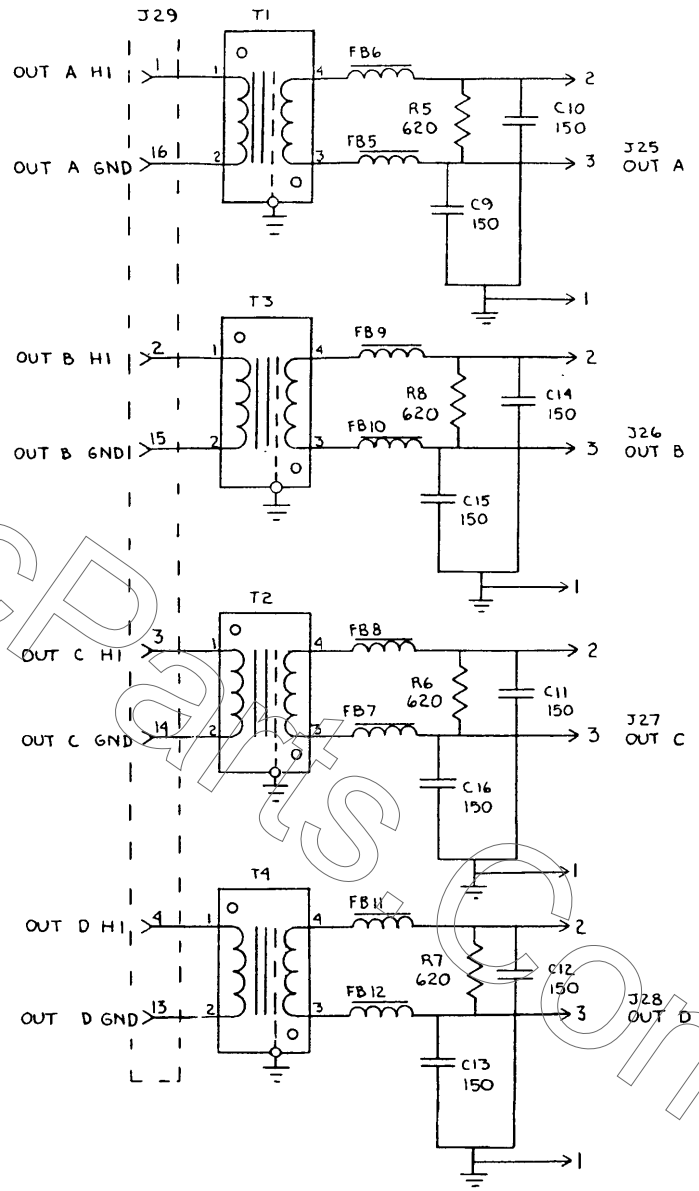
Ircon

SCHEMATIC, OUTPUT BOARD, 224

SIZE	FSCM NO.	DWG. NO.	REV.
		060-01322-C	1

SCALE NA SHEET





REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.	CORRECT LINES TO PIN1, J25-J28. REVERSE HI & LO INPUTS.	8-6-79	

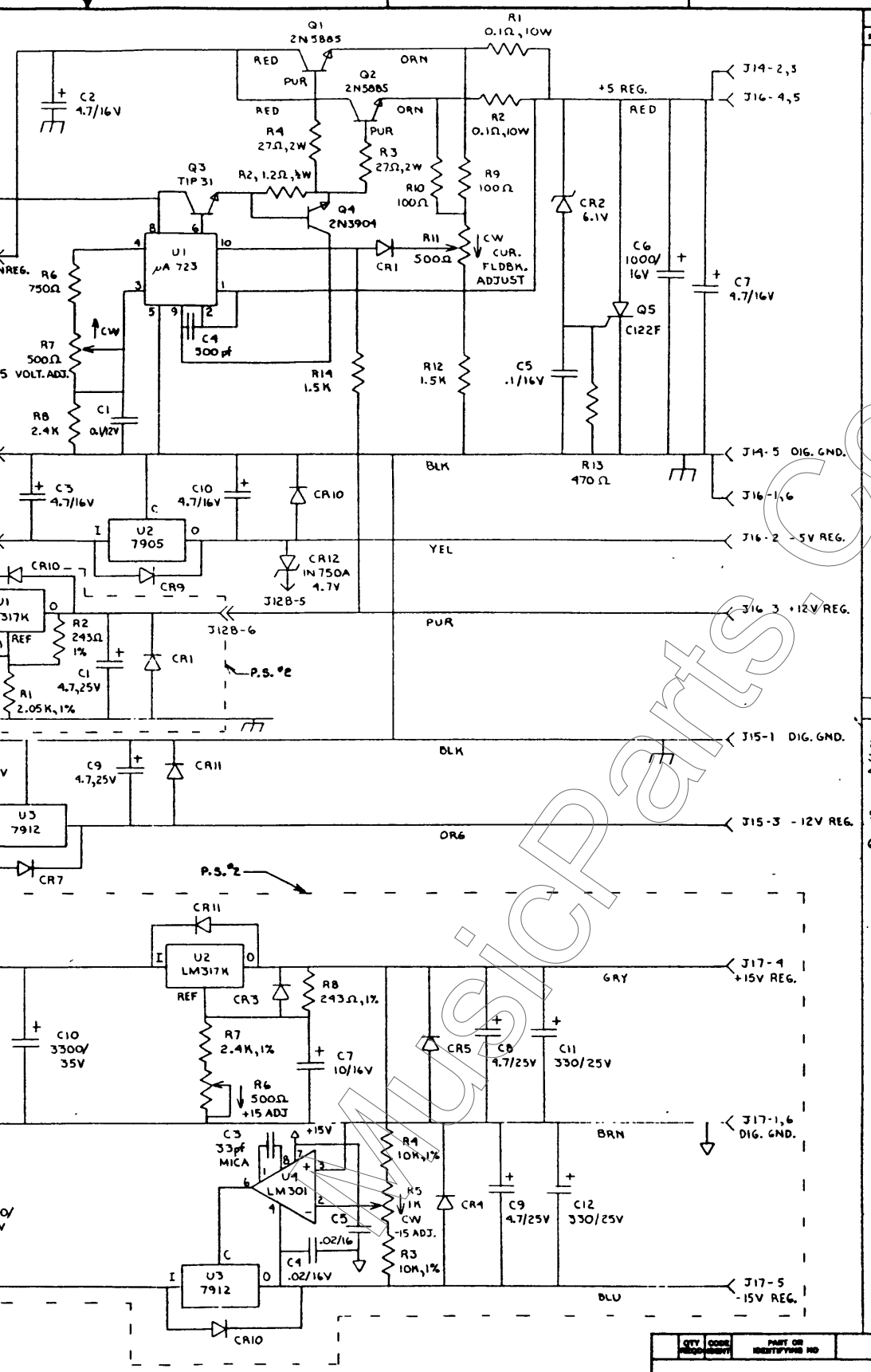
NOTES

1. ALL RESISTORS IN OHMS
2. ALL CAPACITORS IN PF
3. J29 - ANSLEY #609-M161 MASS TERM.
4. J23, J24 IS XLR-D3F
   J25-J28 IS XLR-D3M

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO.		lexicon
	APPROVALS	DATE	XFORMER BOARD
MATERIAL	DRAWN JAG	1-3-79	
	CHECKED		SIZE C · FSCM NO. · DWG. NO. 060-01359-C · REV. 1
NEXT ASSY · USED ON	FINISH	ISSUED C13	8-6-79
APPLICATION	DO NOT SCALE DRAWING		SCALE N.A. · SHEET 1 OF 1



REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1	WAS J15-2, NOW J15-1, WAS J15-1, NOW J15-3; +15V WIRE WAS BLU, NOW GRY; -15V WIRE WAS GRY, NOW BLU	7-18-79	
2	CORRECT POLARITY ON CR3	8-5-79	
J.	CORRECT FAN CONN.	8-15-79	

NOTES

1. RESISTORS 5%, ¼W UNLESS OTHERWISE IND.
2. CAPACITORS IN μf UNLESS OTHERWISE IND.
3. DIODES ARE IN5404 UNLESS OTHERWISE IND.
4. ANALOG GND. ⏚ CHASSIS GND. ⏚ DIGITAL GND.
5. AC WIRING & POWER SUPPLY #1 & 2 ARE ENCLOSED BY DOTTED BOXES; ALL ELSE LIES ON P.S. #3.
6. SEE LEXICON DWG. # 080-01611, ASSEMBLY, POWER SUPPLY FOR SEMICONDUCTOR LOCATIONS AND CONN. IDENTIFICATION.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

NEXT ASSY	224
APPLICATION	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN PMG	6-18-79
CHECKED CB	6-20-79
ISSUED	

lexicon

SCHEMATIC, POWER SUPPLY

SIZE D | FSCM NO. | DWG. NO. 060-01324-D | REV. 1

SCALE NA | SHEET 1 OF 1