Application Note AN3101-01: 1KM as an AES/EBU transmitter

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Introduction

The AES/EBU standard describes a digital serial method of stereo audio data transmission, using a physical transmission medium of a differential pair. The format provides many error-checking capabilities, including three precise preambles, transitions at every bit boundary, validity and parity bits with each channel's sample, and a CRC code for every block of 192 stereo samples or frames. There are also provisions for copyright protection. The format is:

4-bit Preamble,
4-bit Auxiliary Data or Least Significant Bits for audio data over 20 bits,
20-bit Audio Data, least significant bit first,
1-bit Validity, active low,
1-bit User Data,
1-bit Channel Status Data,
1-bit Parity, to make even parity with all preceding except preamble,
followed by the same bit assignments for a second channel.

The channel status data is accumulated over 192 frames, and includes, among other things, the copyright protection features, emphasis and word length information, and the CRC. The data is "Biphase-Mark", also known as "FM". There's a transition at the edge of every bit cell, and if the data bit is 1 there's a transition at the center also.

Algorithm

This application note describes a program to make the DSP-1K act as an AES/EBU transmitter. Stereo Audio Data is taken in on IN0, User Data is taken in on IN1, Channel Status Data in taken in on IN2. Data is assumed always valid, so the Validity bit is always set low. AES/EBU (non-differential) is transmitted on OUT0. OUT1 provides a synchronization pulse which rises shortly before the start of a new block and remains high for a frame period. Channel Status bits are provided to the DSP-1K in a serial stream and sampled just before they are transmitted. The right (second) Channel Status echoes the left; it is not independently sampled. The user does not have to provide the CRC bits; the DSP-1K will calculate them. Due to the fact that the DSP-1K does not have an XOR instruction, CRC accumulation is difficult, and consequently the CRC is calculated only for the left channel. Copyright Data is in the Channel Status bits. **IT IS THE RESPONSIBILITY OF ANY DESIGNER OF AES/EBU EQUIPMENT TO MAKE SURE THAT THE EQUIPMENT IS DESIGNED IN COMPLIANCE WITH THE LAW.**

The audio data is held in addresses $400 and $401. Parity need not be accumulated because with even parity and biphase mark the parity bit transition is always to zero. Output status is saved in $404 (bit 20). CRC is accumulated in bits 16-9 of $405, with bit 9 holding the "most significant" CRC bit. The frame count in each block is maintained in $406 bits 19-12. In $407 bit 20 is temporary storage for the current Channel Status bit. 24 bit audio data is assumed. Control Word 0, bits 1-0 need to be set to 11 to enable 24 bit I/O.

Source Code

```
I#  INSTRUCTION          COMMENT
0   1MC   0x3FD1C0 0x406  ;frame number (bits 19-12) - 185        START LAST FRAME'S CRC
1   SKIP  !N 0xB           ;skip if last 8 blocks
2   CM    1.0 0x405          ;existing CRC in 16-9
3   CMA   0x000080 0x407     ;add Channel Status bit (20->9) from last frame
4   ANDC  0x0000200          ;isolate bit 9 to create XOR
5   C     !Z 0x0240A00       ;for CRC 8-4-3-2-0, bits 21-9
6   XCM   0x101000 0x405     ;save to-be-XORd to B; CRC(16-9) -> acc(18-11),acc(10-3)
7   ANDC  0x00552A8          ;mask even bits 18-11, odd bits 10-3
8   CAB   4.0                ;add in saved bits & move up to acc 20-13 and 12-5. 21 also
9   ANDC  0x0354AA0          ;21-5. Zeroes mask out potential carries, leaving only XORs
A   CAD   0x101000 0.0       ;times hexadecimal 4.04 merges fields. 15-7 of interest now
B   CAD   2.0 0.0            ;shift result into 16-8
C   SKIP  5                 ;past code for last 8 blocks
D   CM    0x040000 0x405     ;get existing CRC
E   ANDC  0x0000200          ;mask for bit 9
F   C     !Z 0x0100000       ;if CRC bit was 1, set bit 20
10  SCA   1.0 0x407          ;save new Channel Status bit. This is a CRC bit.
11  CM    0.5 0x405          ;get CRC; shift right 1
12  ANDC  0x001FE00        ;mask for CRC field, bits 16-9. (Drop bit 8)
13  SCA   0.0 0x405        ;save new CRC; zero the accumulator
14  SKIP  2
15  SKIP  1
16  SKIP  0
17  SCA   1.0 0x421        ;transmit preamble transition
18  CM    1.0 0x406        ;read frame number
19  SKIP  !Z 3
1A  C     0x001FE00        ;frame 0: initialize CRC to all ones
1B  SCA   1.0 0x405        ;save new CRC
1C  SKIP  0
1D  CM    1.0 0x406        ;frame count
1E  C     Z 0x0100000      ;bit 20 is 1 iff frame count is 0 (Preamble Z)
1F  SCA   1.0 0x421        ;preamble transition
20  SKIP  5
; -----------
26  C     0                ;always 0
27  SCA   1.0 0x421        ;preamble transition
28  SKIP  4
; -----------
2D  CM    1.0 0x06         ;frame count
2E  C     !Z 0x0100000     ;bit 20 is 1 iff frame count is not 0 (Preamble X)
2F  SCA   1.0 0x421        ;preamble transition
30  SKIP  5
; -----------
36  C     0                ;always 0
37  SCA   1.0 0x421        ;preamble transition
38  SKIP  5
; -----------                                      START LEFT AUDIO OUT
3E  C     0x0100000        ;always 1
3F  SCA   1.0 0x421        ;first bit cell edge transition
40  SKIP  1
41  SKIP  0
42  CM    1.0 0x410        ;get left audio data
43  SCA   1.0 0x400        ;save
44  ANDC  0x0000001        ;test LSB
45  C     Z 0x0100000      ;transition will be to zero if bit is 1
46  SCA   1.0 0x404        ;save output status
47  SCA   1.0 0x421        ;put out potential transition
48  C     Z 0x0100000      ;1 in bit 20 if LSB is 1
49  SKIP  2
; -----------
```

```
4C  CM    1.0 0x404         ;get output status
4D  C     Z 0x0100000       ;0->1 or 1->0
4E  SCA   1.0 0x404         ;save output status to 404
4F  SCA   1.0 0x421         ;transmit bit edge transition
50  CM    1.0 0x400         ;get audio data
51  ANDC  0x0000002         ;test 2nd LSB
52  C     !Z 0x0100000      ;if bit was 1, set bit 20 to 1
53  CMA   1.0 0x404         ;acc + output status yields XOR in bit 20
54  ANDC  0x0100000         ;isolate the XORd bit
55  SCA   1.0 0x404         ;save output status
56  SKIP  0
57  SCA   1.0 0x421         ;send potential output transition
58  SKIP  3
59  SKIP  2
5A  SKIP  1
5B  SKIP  0
; -----------  REPEAT 4C THROUGH 5B 22 TIMES, EACH TIME REPLACING INSTRUCTION 51 WITH AN
; -----------  INSTRUCTION TO CHECK ONE BIT HIGHER THAN THE LAST TIME. (NOT SHOWN)
1BC CM    1.0 0x404         ;get output status
1BD C     Z 0x0100000       ;0->1 or 1->0
1BE SCA   1.0 0x404         ;save output status
1BF SCA   1.0 0x421         ;send bit edge transition
; -----------        This is validity bit, always=0. No output status change.
; -----------        Use the free time to choose an output for the Channel Status bit
1C0 CM    1.0 0x406         ;get frame count in bits 19-12
1C1 1AC   0xFF48000         ;add -184 (referenced to bit 12) to frame count
1C2 SKIP  !N 3              ;
1C3 CM    0.25 0x419           ;get IN2 data and shift down to bit 20
1C4 ANDC  0x0100000            ;isolate bit 20
1C4 SKIP  3                   ;
1C5 CM    1.0 0x405            ;get the precalculated CRC word. Current bit is 9
1C6 ANDC  0x0000200            ;isolate the current bit
1C7 C     !Z 0x0100000         ;move to bit 20
1C8 SCA   1.0 0x407         ;save Channel Status bit for use at 1E3 and 3E3
1C9 SKIP  2
; -----------
1CC CM    1.0 0x404         ;get output status
1CD C     Z 0x0100000       ;0->1 or 1->0
1CE SCA   1.0 0x404         ;save output status
1CF SCA   1.0 0x421         ;send bit edge transition         START USER BIT
1D0 CM    0.5 0x419         ;get input and shift down 1 bit
1D1 ANDC  0x0100000         ;mask for User bit
1D2 CMA   1.0 0x404         ;acc + output status yields XOR in bit 20
1D3 ANDC  0x0100000         ;isolate the XORd bit
1D4 SCA   1.0 0x404         ;save the output status
1D5 SKIP  1
1D6 SKIP  0
1D7 SCA   1.0 0x421         ;send the user bit transition
1D8 SKIP  3
; -----------
1DC CM    1.0 0x404         ;get output status
1DD C     Z 0x0100000       ;0->1 or 1->0
1DE SCA   1.0 0x404         ;save output status
1DF SCA   1.0 0x421         ;send bit edge transition         START CHANNEL STATUS BIT
1E0 SKIP  2
; -----------
1E3 CM    1.0 0x407         ;get Channel Status bit
1E4 CMA   1.0 0x404         ;acc + output status yields XOR in bit 20
1E5 ANDC  0x0100000         ;isolate XORd bit
1E6 SCA   1.0 0x404         ;save the output status
1E7 SCA   1.0 0x421         ;send the potential Channel Status bit transition
1E8 SKIP  3
; -----------
1EC CM    1.0 0x404         ;get output status
1ED C     Z 0x0100000       ;0->1 or 1->0
1EE SCA   1.0 0x404         ;save output status
1EF SCA   1.0 0x421         ;send bit edge transition
1F0 SKIP  5
; -----------
1F6 C     0                 ;0->acc.  Because parity=even and preamble starts high,
1F7 SCA   1.0 0x421         ;the last transition (parity) is always to zero.
1F8 SKIP  5
; -----------
```

```
1FE C     0x0100000
1FF SCA   1.0 0x421         ;send preamble start
200 SKIP  0x15
; -----------
216 C     0
217 SCA   1.0 0x421         ;send preamble transition
218 SKIP  0xD
; -----------
226 C     0x0100000
227 SCA   1.0 0x421         ;send preamble Y (right channel) transition
228 SKIP  5
; -----------
22E C     0
22F SCA   1.0 0x421         ;send preamble Y (right channel) transition
230 SKIP  4
; -----------
235 C     0x0100000
236 SCA   1.0 0x404         ;save output status
237 SCA   1.0 0x421         ;send first data bit edge transition
238 SKIP  5
; -----------                                          START RIGHT CHANNEL DATA
23E C     0x0100000         ;always 1
23F SCA   1.0 0x421         ;first bit cell edge transition
240 SKIP  1
241 SKIP  0
242 CM    1.0 0x411         ;get right audio data
243 SCA   1.0 0x401         ;save
244 ANDC  0x0000001         ;test LSB
245 C     Z 0x0100000       ;transition will be to zero if bit is 1
246 SCA   1.0 0x404         ;save output status
247 SCA   1.0 0x421         ;put out potential transition
248 C     Z 0x0100000       ;1 in bit 20 if LSB is 1
249 SKIP  2
; -----------
24C CM    1.0 0x404         ;get output status
24D C     Z 0x0100000       ;0->1 or 1->0
24E SCA   1.0 0x404         ;save output status to 404
24F SCA   1.0 0x421         ;transmit bit edge transition
250 CM    1.0 0x401         ;get audio data
251 ANDC  0x0000002         ;test 2nd LSB
252 C     !Z 0x0100000      ;if bit was 1, set bit 20 to 1
253 CMA   1.0 0x404         ;acc + output status yields XOR in bit 20
254 ANDC  0x0100000         ;isolate the XORd bit
255 SCA   1.0 0x404         ;save output status
256 SKIP  0
257 SCA   1.0 0x421         ;send potential output transition
258 SKIP  3
259 SKIP  2
25A SKIP  1
25B SKIP  0
; -----------  REPEAT 24C THROUGH 25B 22 TIMES, EACH TIME REPLACING INSTRUCTION 251 WITH
; -----------  AN INSTRUCTION TO CHECK ONE BIT HIGHER THAN THE LAST TIME. (NOT SHOWN)
3BC CM    1.0 0x404         ;get output status
3BD C     Z 0x0100000       ;0->1 or 1->0
3BE SCA   1.0 0x404         ;save output status
3BF SCA   1.0 0x421         ;send bit edge transition
3C0 SKIP  0xB
; -----------        This is validity bit, always=0. No output status change.
3CC CM    1.0 0x404         ;get output status
3CD C     Z 0x0100000       ;0->1 or 1->0
3CE SCA   1.0 0x404         ;save output status
3CF SCA   1.0 0x421         ;send bit edge transition         START USER BIT
3D0 CM    0.5 0x419         ;get input and shift down 1 bit
3D1 ANDC  0x0100000         ;mask for User bit
3D2 CMA   1.0 0x404         ;acc + output status yields XOR in bit 20
3D3 ANDC  0x0100000         ;isolate the XORd bit
3D4 SCA   1.0 0x404         ;save the output status
3D5 SKIP  1
3D6 SKIP  0
3D7 SCA   1.0 0x421         ;send the user bit transition
3D8 SKIP  3
; -----------
```

```
3DC CM    1.0 0x404         ;get output status
3DD C     Z 0x0100000       ;0->1 or 1->0
3DE SCA   1.0 0x404         ;save output status
3DF SCA   1.0 0x421         ;send bit edge transition         START CHANNEL STATUS BIT
3E0 SKIP  2
; -----------
3E3 CM    1.0 0x407         ;get Channel Status bit
3E4 CMA   1.0 0x404         ;acc + output status yields XOR in bit 20
3E5 ANDC  0x0100000         ;isolate XORd bit
3E6 SCA   1.0 0x404         ;save the output status
3E7 SCA   1.0 0x421         ;send the potential Channel Status bit transition
3E8 SKIP  3
; -----------
3EC CM    1.0 0x404         ;get output status
3ED C     Z 0x0100000       ;0->1 or 1->0
3EE SCA   1.0 0x404         ;save output status
3EF SCA   1.0 0x421         ;send bit edge transition
3F0 SKIP  3
; -----------
3F4 1MC   0x3FD040 0x406     ;frame count -191
3F5 C     Z 0x0200000       ;
3F6 SCA   0.0 0x422         ;send 1 to OUT1 if new block about to start, else 0. 0->acc.
3F7 SCA   1.0 0x421         ;Even parity => last transition (parity) is always to zero.
3F8 1MC   0x000040 0x406    ;sample count + 1  (sample count LSB is bit 12)
3F9 ANDC  0x00FF000         ;limit range to 0-255
3FA X1AC  0xFF40000         ;acc->B, acc-192->acc
3FB C     N 1.0             ;if result of -192 was negative, 1.0->acc, else 0.0->acc
3FC BAC   1.0               ;if 1.0 in acc, restore B to acc, else 0->acc
3FD SCA   1.0 0x406         ;save new sample count
3FE C     0x0100000         ;prepare data for preamble's first edge
3FF SCA   1.0 0x421         ;transmit preamble start to OUT0
; -----------    START AGAIN AT INSTRUCTION 0
```

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Application note revised March, 2005