AppNote AN3101-09: S/Mux Transmitter for ADAT® Optical Protocol

By Shultz Wang

Introduction

The ADAT® Optical protocol allows the transmission of eight 24-bit channels at a sample rate of 48kHz down a single connection. With the advent of 96kHz sampling rates, it became necessary to expand the protocol to allow the transmission of higher data rates down the same pipeline and thus retain some backwards compatibility. The February 2001 addendum to the ADAT® protocol defined the changes which allowed this expansion. This method of transmitting four 24-bit 96kHz channels down the same ADAT® pipeline has been dubbed S/Mux by the audio community.

After an examination of the addendum, it became clear that an S/Mux transmitter may be implemented on a DSP-1K by directly reading 96kHz data on its input pins, reconstructing the bitstreams, and sending out the reordered channels on its output pins for direct connection to an OptoGen.

Algorithm

Pseudocode:

```
Repeat (4) {
        Repeat (24) {
                Direct read input pin
                Shift read value to correct location in word
                Add to store register i
        }
        Wait for end of 96kHz channel frame
}
Output4 channels
Clear store registers
```

The DSP-1K assembly code basically follows the pseudocode above, with the addition of NOPs padding for timing purposes. The assembly code is written such that it takes in 4 channels of 96kHz data on the pins IN0 and IN1, and the output pins OUT0..OUT3 may be connected directly to pins IN1/2..IN7/8 on an OptoGen for an instant S/Mux transmitter solution.

* Note: Since the DSP-1K takes in a 48kHz clock rate, it will be up to the user to provide it a 48kHz clock with a correct phase relation to the 96kHz data. Both the DSP-1K and the OptoGen should be fed the same 48kHz wordclock to keep them synchronized. Be sure to set the USER2 pin of the OptoGen high to indicate the use of S/Mux mode.

Source code

```
; Application Note AN3101-09: S/Mux transmitter for ADAT® optical protocol
;                 By Shultz Wang

; Version 1.0 - Oct 16 2003

; Delay read until middle of 6MHz bitclock for 96kHz datastream
cb    0.0               ; NOP
cb    0.0               ; NOP
cb    0.0               ; NOP
cb    0.0               ; NOP


; First quarter of 48kHz wordclock

cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0400000                ; AND out In0 pin value at bit 22
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $400        ; Save new $Ch0L0
cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0800000                ; AND out In1 pin value at bit 23
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $401        ; Save new $Ch1L0

cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   1.0         $400  ; Right shift In0 pin value 0 bits, add $Ch0L0
sca   1.0         $400
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.5         $401  ; Right shift In1 pin value 1 bits, add $Ch1L0
sca   1.0         $401

cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   0.5         $400  ; Right shift 1 bits
sca   1.0         $400
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.25        $401  ; Right shift 2 bits
sca   1.0         $401

            ; Repeat the following block 21 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    $100000*    $419  ; Right shifted -2 bits
andc  $0400000*         ; Bit 22
cam   0.25        $400  ; Right shift 2 bits
sca   1.0         $400
cm    $100000*    $419  ; Right shifted -2 bits
andc  $0800000*         ; Bit 23
cam   0.125       $401  ; Right shift 3 bits
sca   1.0         $401
            ; End repeated block

            ; Repeat the following NOP 64 times (not shown)
cb    0.0               ; NOP
```

```
; Second quarter of 48kHz wordclock

cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0400000                ; AND out In0 pin value at bit 22
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $402        ; Save new $Ch0R0
cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0800000                ; AND out In1 pin value at bit 23
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $403        ; Save new $Ch1R0

cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   1.0         $402  ; Right shift In0 pin value 0 bits, add $Ch0R0
sca   1.0         $402
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.5         $403  ; Right shift In1 pin value 1 bits, add $Ch1R0
sca   1.0         $403

cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   0.5         $402  ; Right shift 1 bits
sca   1.0         $402
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.25        $403  ; Right shift 2 bits
sca   1.0         $403

            ; Repeat the following block 21 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    $100000*    $419  ; Right shifted -2 bits
andc  $0400000*         ; Bit 22
cam   0.25        $402  ; Right shift 2 bits
sca   1.0         $402
cm    $100000*    $419  ; Right shifted -2 bits
andc  $0800000*         ; Bit 23
cam   0.125       $403  ; Right shift 3 bits
sca   1.0         $403
            ; End repeated block

            ; Repeat the following NOP 64 times (not shown)
cb    0.0               ; NOP


; Third quarter of 48kHz wordclock

cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0400000                ; AND out In0 pin value at bit 22
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $404        ; Save new $Ch0L1
cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0800000                ; AND out In1 pin value at bit 23
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $405        ; Save new $Ch1L1

cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   1.0         $404  ; Right shift In0 pin value 0 bits, add $Ch0L1
sca   1.0         $404
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.5         $405  ; Right shift In0 pin value 1 bits, add $Ch0L1
sca   1.0         $405
```

```
cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   0.5         $404  ; Right shift 1 bits
sca   1.0         $404
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.25        $405  ; Right shift 2 bits
sca   1.0         $405

            ; Repeat the following block 21 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    $100000*    $419  ; Right shifted -2 bits
andc  $0400000*         ; Bit 22
cam   0.25        $404  ; Right shift 2 bits
sca   1.0         $404
cm    $100000*    $419  ; Right shifted -2 bits
andc  $0800000*         ; Bit 23
cam   0.125       $405  ; Right shift 3 bits
sca   1.0         $405
            ; End repeated block

            ; Repeat the following NOP 64 times (not shown)
cb    0.0               ; NOP


; Fourth quarter of 48kHz wordclock

cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0400000                ; AND out In0 pin value at bit 22
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $406        ; Save new $Ch0R1
cm    $100000     $419        ; Read pin values right shifted -2 bits
andc  $0800000                ; AND out In1 pin value at bit 23
c     !z          $f800000    ; Set sign bits if not zero
sca   1.0         $407        ; Save new $Ch1R1

cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   1.0         $406  ; Right shift In0 pin value 0 bits, add $Ch0R1
sca   1.0         $406
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.5         $407  ; Right shift In1 pin value 1 bits, add $Ch1R1
sca   1.0         $407


cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   0.5         $406  ; Right shift 1 bits
sca   1.0         $406
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.25        $407  ; Right shift 2 bits
sca   1.0         $407
```

```
            ; Repeat the following block 21 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    $100000     $419  ; Right shifted -2 bits
andc  $0400000          ; Bit 22
cam   0.25        $406  ; Right shift 2 bits
sca   1.0         $406
cm    $100000     $419  ; Right shifted -2 bits
andc  $0800000          ; Bit 23
cam   0.125       $407  ; Right shift 3 bits
sca   1.0         $407
            ; End repeated block

; Write to output registers
cm    1.0         $400  ; Read $Ch0L0
sca   0.0         $410  ; Write $Ch0
cm    1.0         $401  ; Read $Ch1L0
sca   0.0         $414  ; Write $Ch4
cm    1.0         $402  ; Read $Ch0R0
sca   0.0         $412  ; Write $Ch2
cm    1.0         $403  ; Read $Ch1R0
sca   0.0         $416  ; Write $Ch6
cm    1.0         $404  ; Read $Ch0L1
sca   0.0         $411  ; Write $Ch1
cm    1.0         $405  ; Read $Ch1L1
sca   0.0         $415  ; Write $Ch5
cm    1.0         $406  ; Read $Ch0R1
sca   0.0         $413  ; Write $Ch3
cm    1.0         $407  ; Read $Ch1R1
sca   0.0         $417  ; Write $Ch7

; Clear storage locations
sca   0.0         $400
sca   0.0         $401
sca   0.0         $402
sca   0.0         $403
sca   0.0         $404
sca   0.0         $405
sca   0.0         $406
sca   0.0         $407
```

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