AppNote AN3101-09: S/Mux Receiver for ADAT® Optical Protocol

By Shultz Wang

Introduction

The ADAT® Optical protocol allows the transmission of eight 24-bit channels at a sample rate of 48kHz down a single connection. With the advent of 96kHz sampling rates, it became necessary to expand the protocol to allow the transmission of higher data rates down the same pipeline and thus retain some backwards compatibility. The February 2001 addendum to the ADAT® protocol defined the changes which allowed this expansion. This method of transmitting four 24-bit 96kHz channels down the same ADAT® pipeline has been dubbed S/Mux by the audio community.

After an examination of the addendum, it became clear that an S/Mux receiver may be implemented on a DSP-1K by reading the reordered channels from an OptoRec on its input pins, reconstructing the bitstreams, and directly writing the 96kHz data on its output pins.

Algorithm

Pseudocode:

```
Repeat (4) {
        Repeat (24) {
                Isolate bit i of channel j
                Direct write bit i to output
        }
}
```

The DSP-1K assembly code basically follows the pseudocode above, with the addition of NOPs padding for timing purposes. The assembly code is written such that it sends out 4 channels of 96kHz data on the pins OUT0 and OUT1, and the input pins IN0..IN3 may be connected directly to pins OUT1/2..OUT7/8 on an OptoRec for an instant S/Mux receiver solution.

* Note: Since the DSP-1K takes in a 48kHz clock rate, it will be up to the user to provide it a 48kHz clock with a correct phase relation to the 96kHz data. Both the DSP-1K and the OptoGen should be fed the same 48kHz wordclock to keep them synchronized. Be sure to check the USER2 pin of the OptoRec to ensure that the received data is indeed in S/Mux mode.

Source code

```
; Application Note AN3101-10: S/Mux receiver for ADAT® optical protocol
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; Delay read until middle of 6MHz bitclock for 96kHz datastream


; First quarter of 48kHz wordclock continued

            ; Repeat the following block 23 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    1.0           $400        ; Read $Ch0L0
andc  $0400000*                 ; AND out bit 22 of $Ch0L0
c     !z            $0100000    ; Set Out0 bit if not zero
xcm   1.0           $404        ; B=Out0, read $Ch1L0
andc  $0400000*                 ; AND out bit 22 of $Ch1L0
c     !z            $0200000    ; Set Out1 bit if not zero
cab   1.0                       ; Combine bits
sca   1.0           $423        ; Write Out1 and Out0
            ; End repeated block

cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
sca   1.0           $423  ; Return output pins to 0

            ; Repeat the following NOP 56 times (not shown)
cb    0.0                 ; NOP


; Second quarter of 48kHz wordclock

            ; Repeat the following block 24 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    1.0           $402        ; Read $Ch0R0
andc  $0800000*                 ; AND out bit 23 of $Ch0R0
c     !z            $0100000    ; Set Out0 bit if not zero
xcm   1.0           $406        ; B=Out0, read $Ch1R0
andc  $0800000*                 ; AND out bit 23 of $Ch1R0
c     !z            $0200000    ; Set Out1 bit if not zero
cab   1.0                       ; Combine bits
sca   1.0           $423        ; Write Out1 and Out0
            ; End repeated block

cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
sca   1.0           $423  ; Return output pins to 0

            ; Repeat the following NOP 56 times (not shown)
cb    0.0                 ; NOP
```

```
; Third quarter of 48kHz wordclock

            ; Repeat the following block 24 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    1.0           $401          ; Read $Ch0L1
andc  $0800000*                   ; AND out bit 23 of $Ch0L1
c     !z            $0100000      ; Set Out0 bit if not zero
xcm   1.0           $405          ; B=Out0, read $Ch1L1
andc  $0800000*                   ; AND out bit 23 of $Ch1L1
c     !z            $0200000      ; Set Out1 bit if not zero
cab   1.0                         ; Combine bits
sca   1.0           $423          ; Write Out1 and Out0
            ; End repeated block

cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
sca   1.0           $423  ; Return output pins to 0

            ; Repeat the following NOP 56 times (not shown)
cb    0.0                 ; NOP


; Fourth quarter of 48kHz wordclock

            ; Repeat the following block 24 times (not shown), each time after
            ; the first right shifting the values marked with an "*" by 1 bit.
cm    1.0           $403          ; Read $Ch0R1
andc  $0800000                    ; AND out bit 23 of $Ch0R1
c     !z            $0100000      ; Set Out0 bit if not zero
xcm   1.0           $407          ; B=Out0, read $Ch1R1
andc  $0800000                    ; AND out bit 23 of $Ch1R1
c     !z            $0200000      ; Set Out1 bit if not zero
cab   1.0                         ; Combine bits
sca   1.0           $423          ; Write Out1 and Out0
            ; End repeated block
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
cb    0.0                 ; NOP
sca   1.0           $423  ; Return output pins to 0

            ; Repeat the following NOP 40 times (not shown)
cb    0.0                 ; NOP

; Read Ch7-0 into registers
cm    1.0           $410
sca   1.0           $400
cm    1.0           $411
sca   1.0           $401
cm    1.0           $412
sca   1.0           $402
cm    1.0           $413
sca   1.0           $403
cm    1.0           $414
sca   1.0           $404
```

```
cm    1.0         $415
sca   1.0         $405
cm    1.0         $416
sca   1.0         $406
cm    1.0         $417
sca   1.0         $407


; First quarter of 48kHz wordclock

cm    1.0         $400        ; Read $Ch0L0
andc  $0800000                ; AND out bit 23 of $Ch0L0
c     !z          $0100000    ; Set Out0 bit if not zero
xcm   1.0         $404        ; B=Out0, read $Ch1L0
andc  $0800000                ; AND out bit 23 of $Ch1L0
c     !z          $0200000    ; Set Out1 bit if not zero
cab   1.0                     ; Combine bits
sca   1.0         $423        ; Write Out1 and Out0
```

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